

Vinafix



QUANTA
COMPUTER

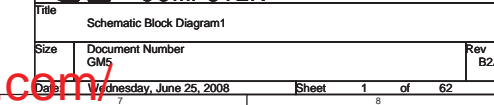



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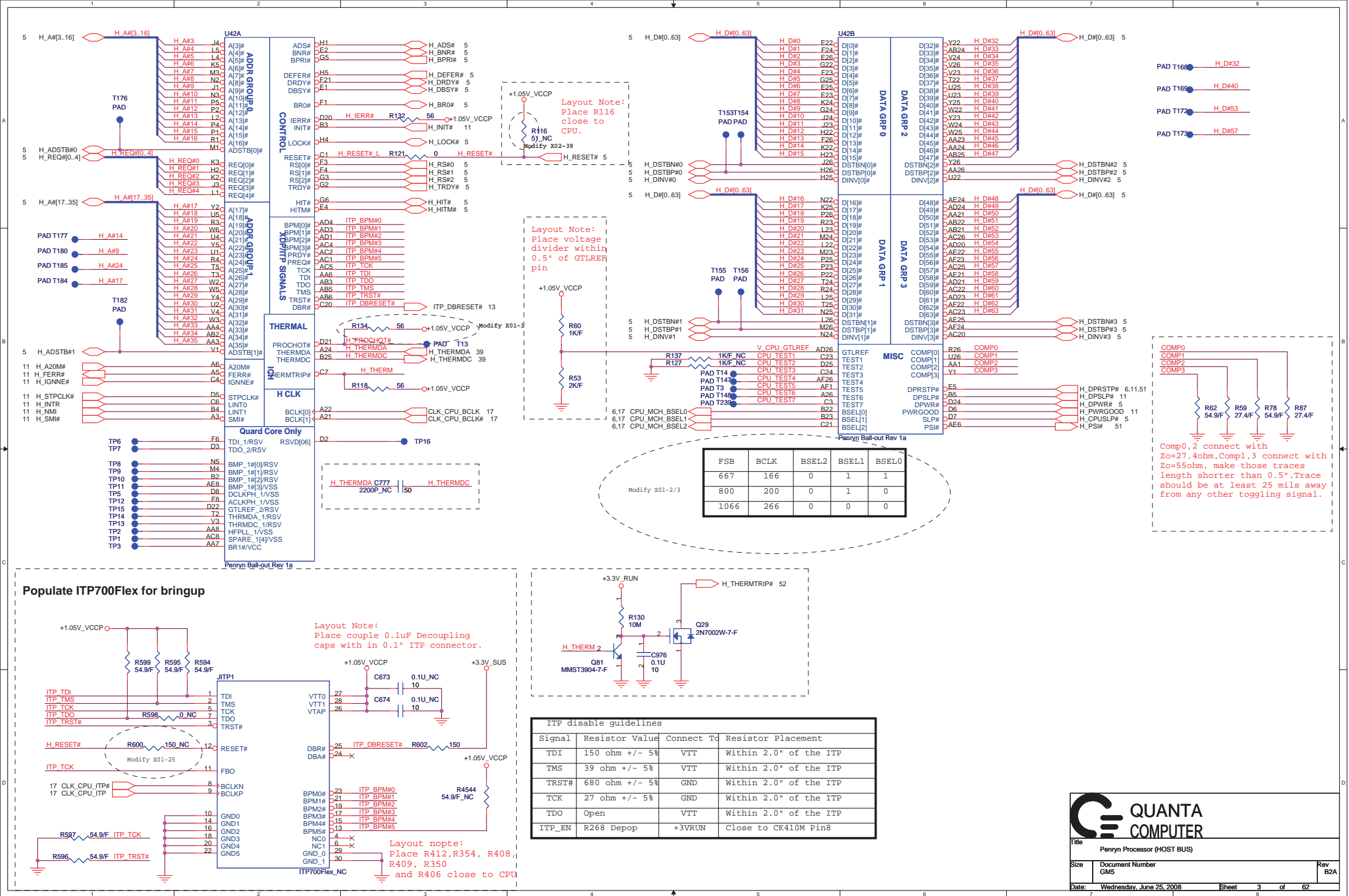
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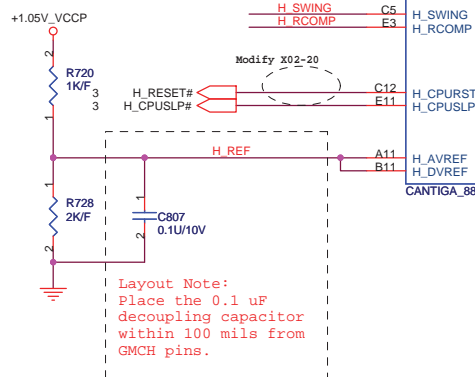
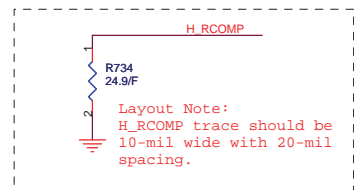
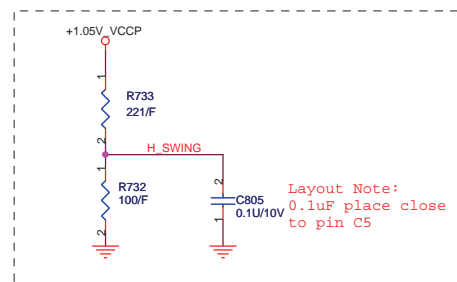
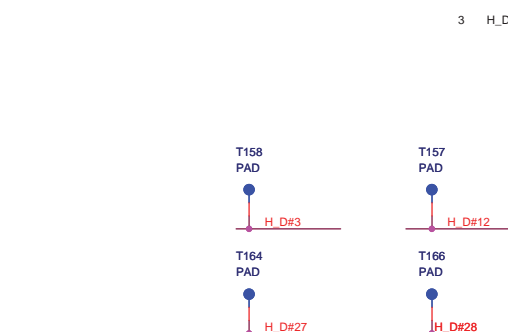
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CANTIGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CANTIGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	

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U45A

H_D#0	F2	H_D# 0
H_D#1	G8	H_D# 1
H_D#2	F8	H_D# 2
H_D#3	E6	H_D# 3
H_D#4	G2	H_D# 4
H_D#5	H6	H_D# 5
H_D#6	H2	H_D# 6
H_D#7	F6	H_D# 7
H_D#8	D4	H_D# 8
H_D#9	H3	H_D# 9
H_D#10	M9	H_D# 10
H_D#11	M11	H_D# 11
H_D#12	J2	H_D# 12
H_D#13	N12	H_D# 13
H_D#14	J6	H_D# 14
H_D#15	P2	H_D# 15
H_D#16	L2	H_D# 16
H_D#17	R2	H_D# 17
H_D#18	N9	H_D# 18
H_D#19	L6	H_D# 19
H_D#20	M5	H_D# 20
H_D#21	J3	H_D# 21
H_D#22	N2	H_D# 22
H_D#23	R1	H_D# 23
H_D#24	N5	H_D# 24
H_D#25	N6	H_D# 25
H_D#26	P13	H_D# 26
H_D#27	N8	H_D# 27
H_D#28	L7	H_D# 28
H_D#29	N10	H_D# 29
H_D#30	M3	H_D# 30
H_D#31	Y3	H_D# 31
H_D#32	AD14	H_D# 32
H_D#33	Y6	H_D# 33
H_D#34	Y10	H_D# 34
H_D#35	Y12	H_D# 35
H_D#36	Y14	H_D# 36
H_D#37	Y7	H_D# 37
H_D#38	W2	H_D# 38
H_D#39	AA8	H_D# 39
H_D#40	Y9	H_D# 40
H_D#41	AA13	H_D# 41
H_D#42	AA9	H_D# 42
H_D#43	AA11	H_D# 43
H_D#44	AD11	H_D# 44
H_D#45	AD10	H_D# 45
H_D#46	AD10	H_D# 46
H_D#47	AD13	H_D# 47
H_D#48	AE12	H_D# 48
H_D#49	AE9	H_D# 49
H_D#50	AA2	H_D# 50
H_D#51	AD8	H_D# 51
H_D#52	AA3	H_D# 52
H_D#53	AD3	H_D# 53
H_D#54	AD7	H_D# 54
H_D#55	AE14	H_D# 55
H_D#56	AE3	H_D# 56
H_D#57	AE3	H_D# 57
H_D#58	AC1	H_D# 58
H_D#59	AC3	H_D# 59
H_D#60	AE11	H_D# 60
H_D#61	AE8	H_D# 61
H_D#62	AG2	H_D# 62
H_D#63	AD6	H_D# 63

HOST

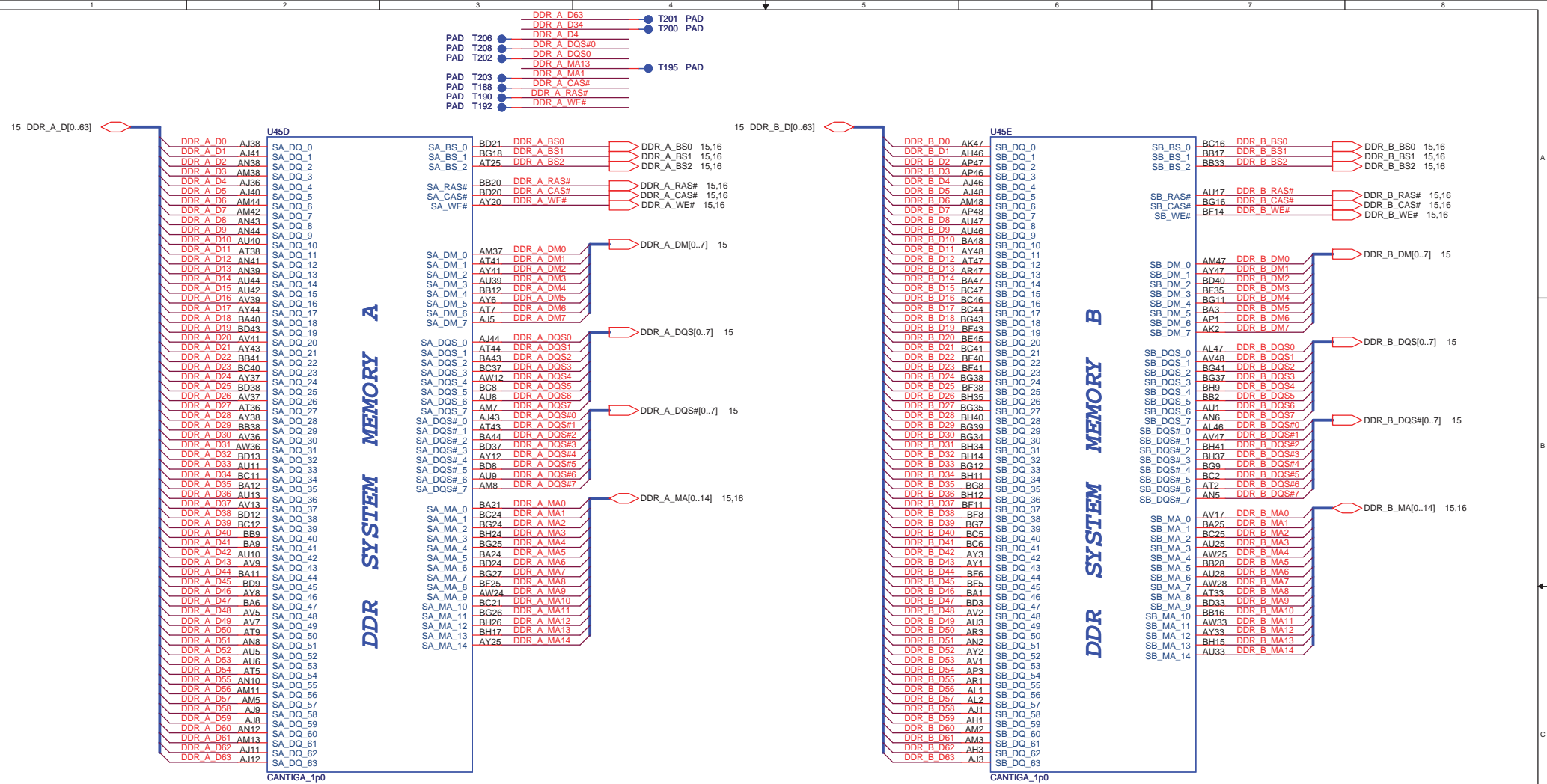
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H_A# 4	C15	H_A#4
H_A# 5	E16	H_A#5
H_A# 6	H13	H_A#6
H_A# 7	C18	H_A#7
H_A# 8	M16	H_A#8
H_A# 9	J13	H_A#9
H_A# 10	P16	H_A#10
H_A# 11	R16	H_A#11
H_A# 12	N17	H_A#12
H_A# 13	M13	H_A#13
H_A# 14	E17	H_A#14
H_A# 15	P17	H_A#15
H_A# 16	G20	H_A#16
H_A# 17	B19	H_A#17
H_A# 18	J16	H_A#18
H_A# 19	E20	H_A#19
H_A# 20	H16	H_A#20
H_A# 21	J20	H_A#21
H_A# 22	L17	H_A#22
H_A# 23	A17	H_A#23
H_A# 24	B17	H_A#24
H_A# 25	L16	H_A#25
H_A# 26	C21	H_A#26
H_A# 27	J17	H_A#27
H_A# 28	H20	H_A#28
H_A# 29	B18	H_A#29
H_A# 30	K17	H_A#30
H_A# 31	B20	H_A#31
H_A# 32	F21	H_A#32
H_A# 33	K21	H_A#33
H_A# 34	L20	H_A#34
H_A# 35		H_A#35

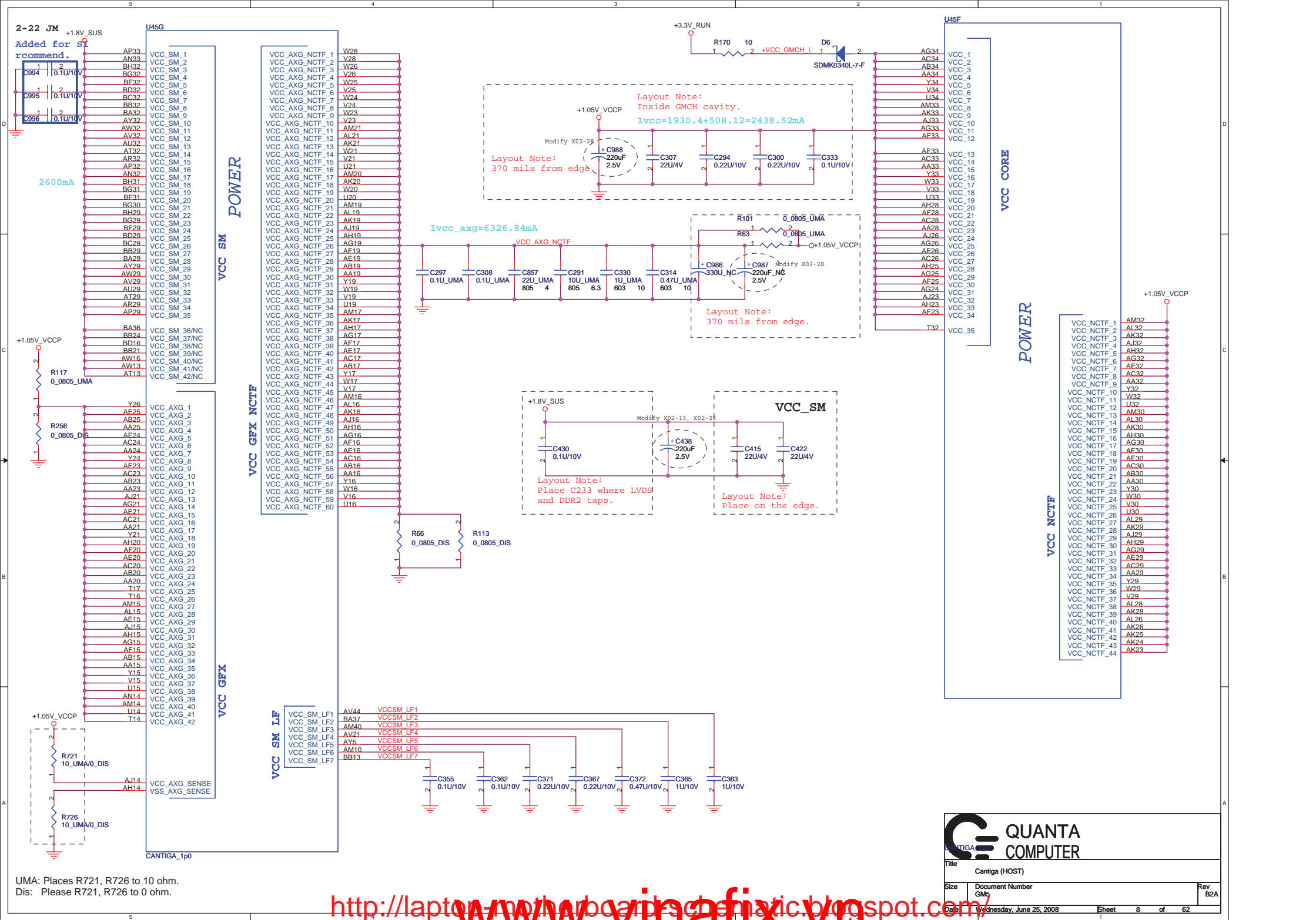
H_ADS#	H12	H_ADS# 3
H_ADSTB# 0	B16	H_ADSTB#0 3
H_ADSTB# 1	G17	H_ADSTB#1 3
H_BNR#	A9	H_BNR# 3
H_BPRI#	F11	H_BPRI# 3
H_BREQ#	G12	H_BREQ# 3
H_DEFER#	E9	H_DEFER# 3
H_DBSY#	B10	H_DBSY# 3
H_DBSY# 3	AH7	H_DBSY# 3
HPLL_CLK	AH6	CLK MCH BCLK 17
HPLL_CLK#	AH6	CLK MCH BCLK# 17
H_DPWR#	J11	H_DPWR# 3
H_DRDY#	E9	H_DRDY# 3
H_HIT#	H8	H_HIT# 3
H_HITM#	E12	H_HITM# 3
H_LOCK#	H11	H_LOCK# 3
H_TRDY#	C9	H_TRDY# 3

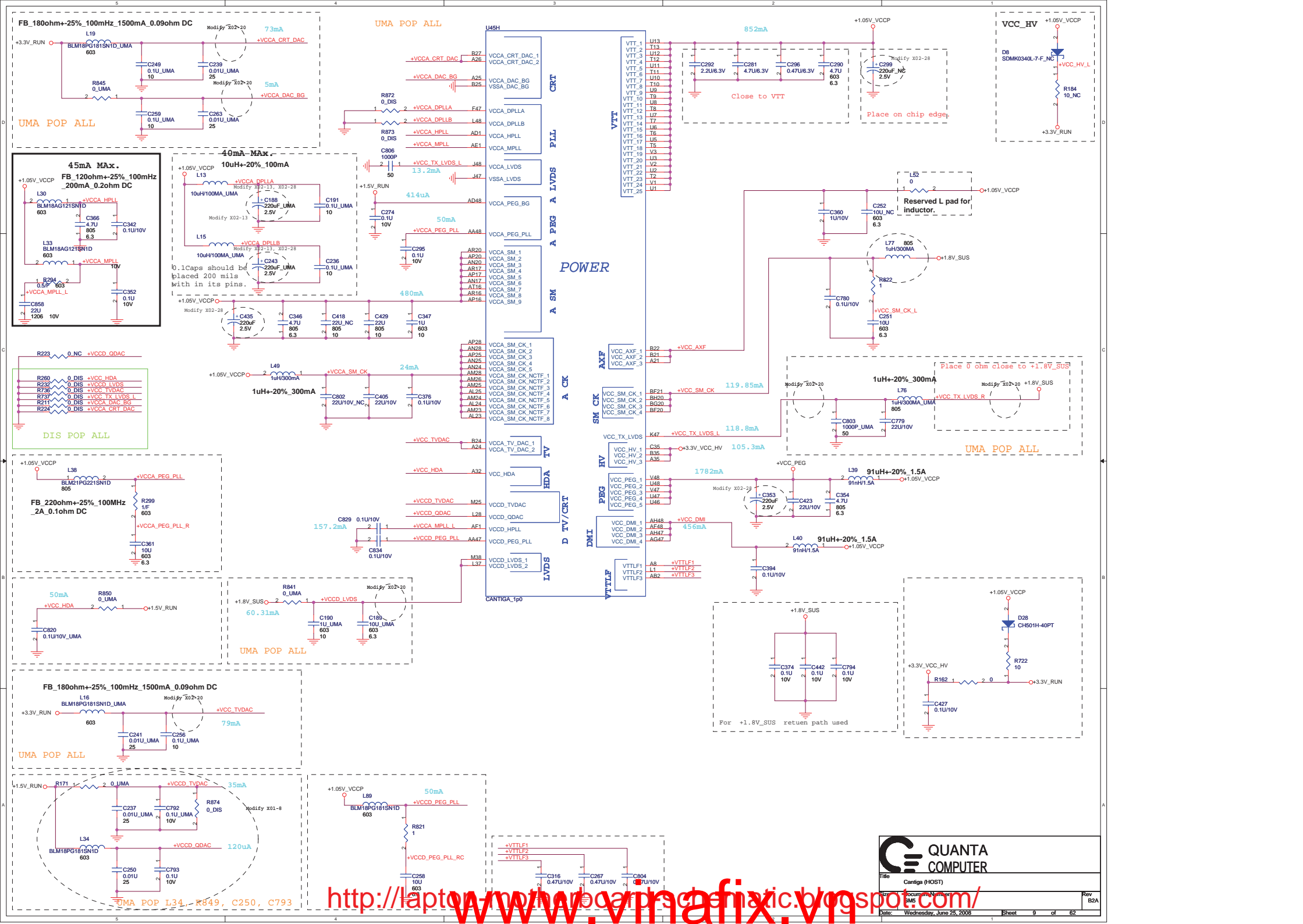
H_DIN# 0	J8	H_DIN#0 3
H_DIN# 1	L3	H_DIN#1 3
H_DIN# 2	Y13	H_DIN#2 3
H_DIN# 3	Y1	H_DIN#3 3
H_DSTBN# 0	L10	H_DSTBN#0 3
H_DSTBN# 1	M7	H_DSTBN#1 3
H_DSTBN# 2	AA5	H_DSTBN#2 3
H_DSTBN# 3	AE6	H_DSTBN#3 3
H_DSTBP# 0	L9	H_DSTBP#0 3
H_DSTBP# 1	M8	H_DSTBP#1 3
H_DSTBP# 2	AA6	H_DSTBP#2 3
H_DSTBP# 3	AE5	H_DSTBP#3 3
H_REQ# 0	B15	H_REQ#0 3
H_REQ# 1	K13	H_REQ#1 3
H_REQ# 2	F13	H_REQ#2 3
H_REQ# 3	B13	H_REQ#3 3
H_REQ# 4	B14	H_REQ#4 3
H_RS# 0	B6	H_RS#0 3
H_RS# 1	F12	H_RS#1 3
H_RS# 2	C8	H_RS#2 3

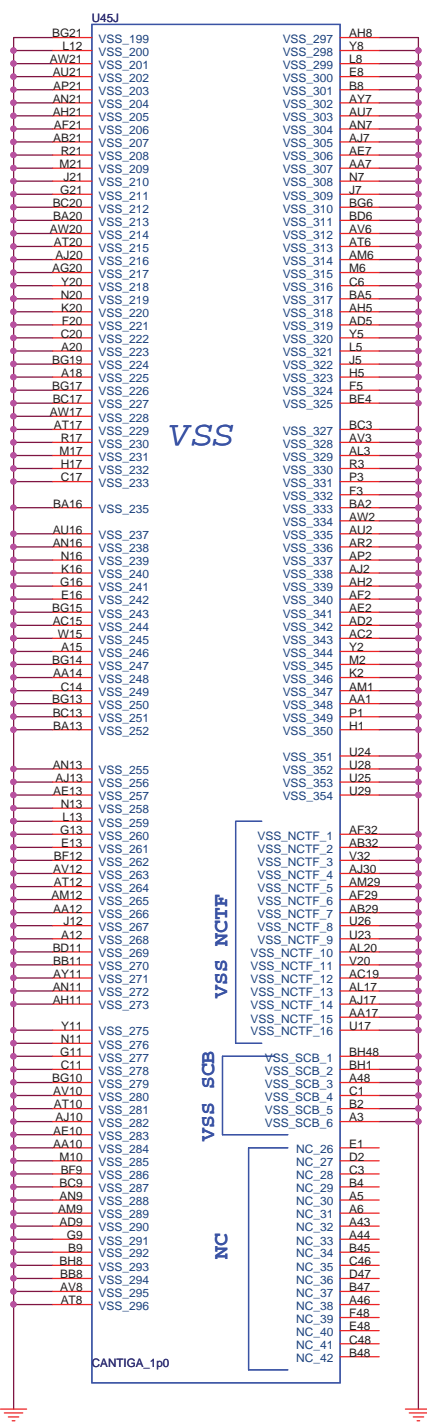
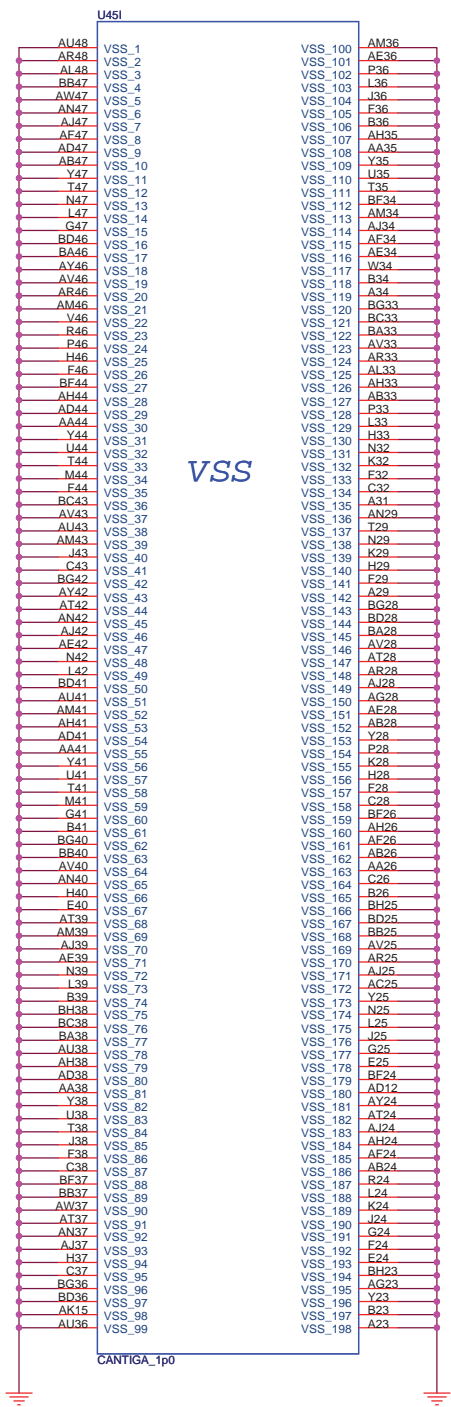



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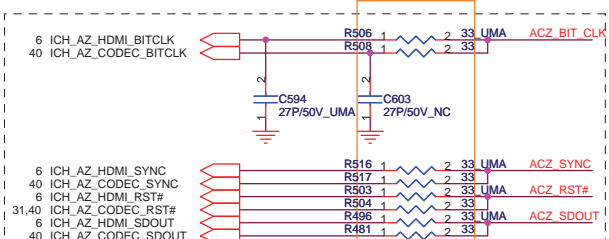
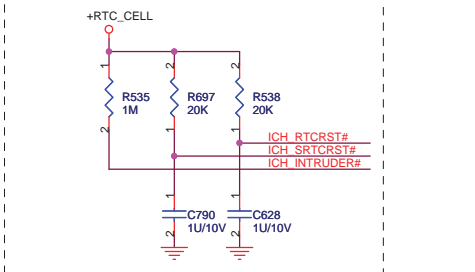
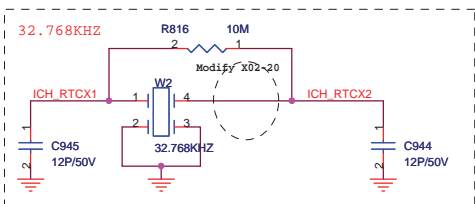




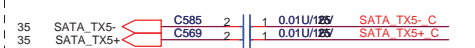
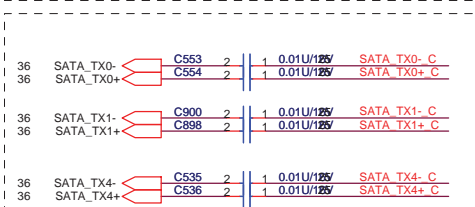
 **QUANTA**
COMPUTER

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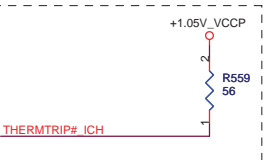
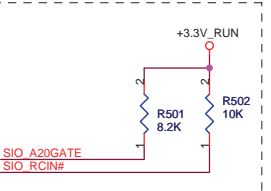
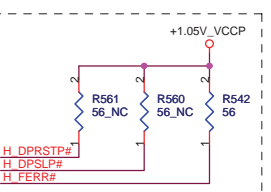
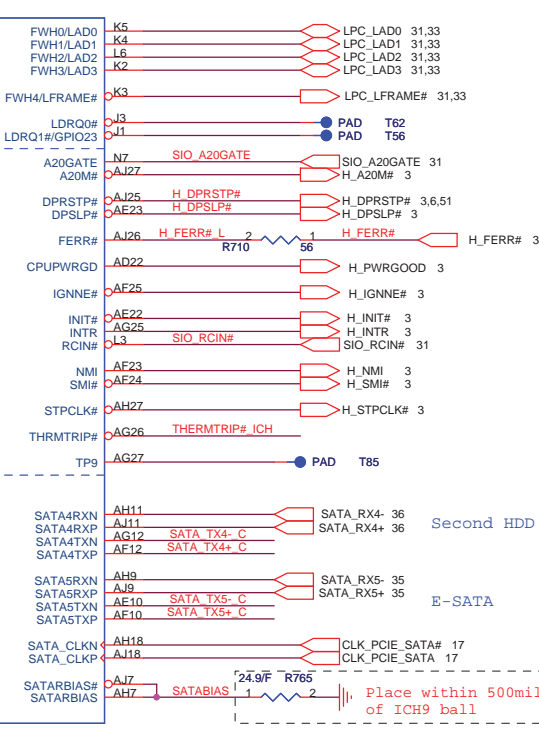
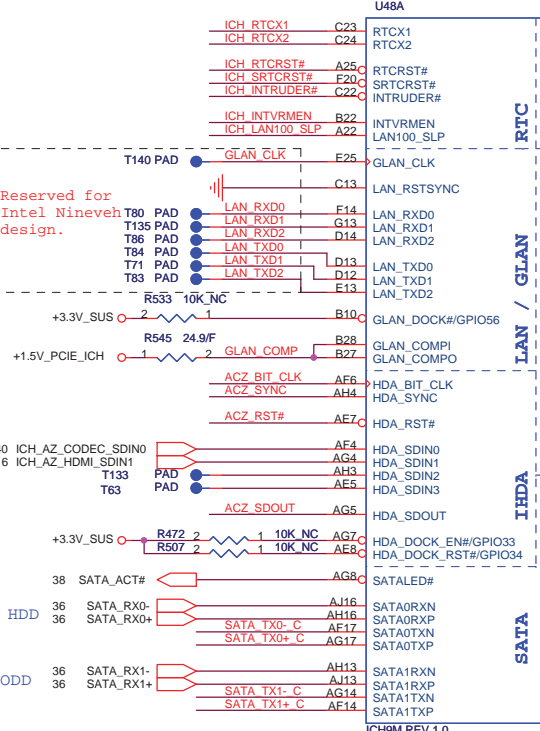
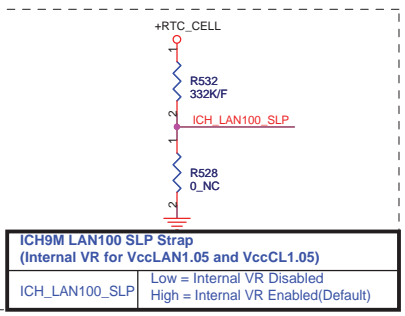
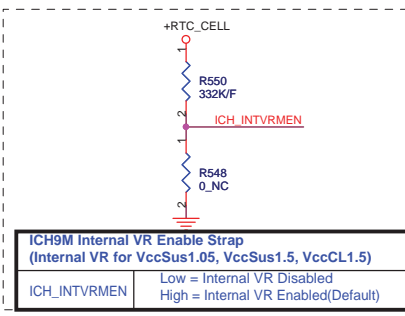
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Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.



Master HDD

SATA ODD

XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

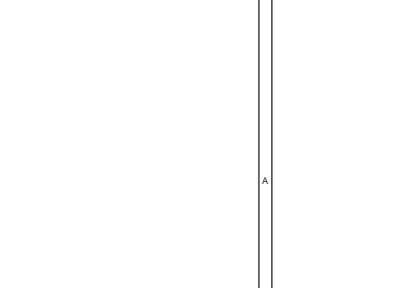
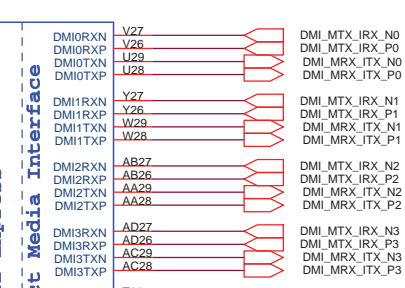
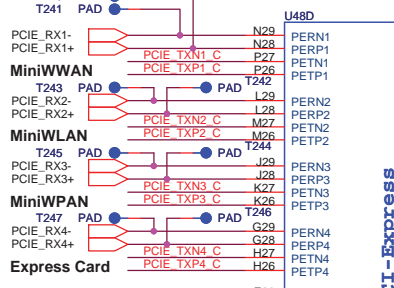
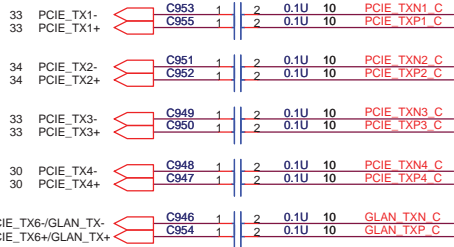
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Title: ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)

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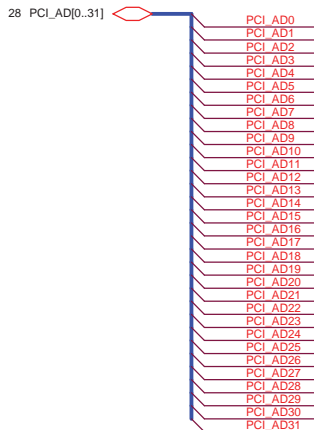
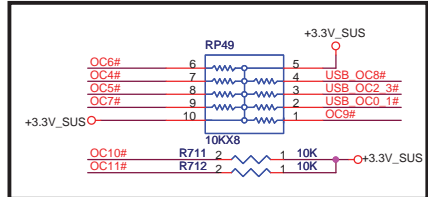
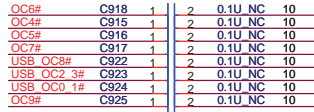
Place TX DC blocking caps close ICH8.

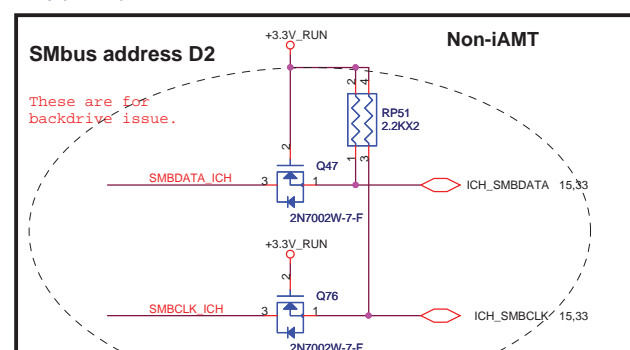
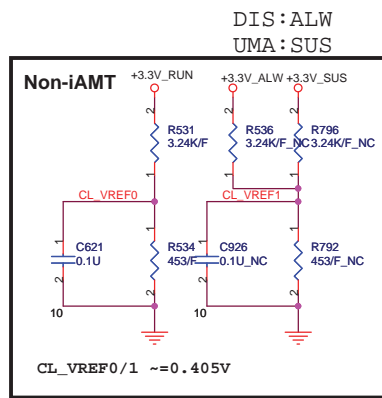
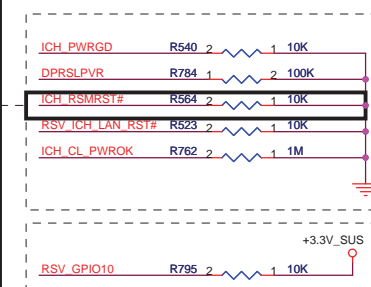
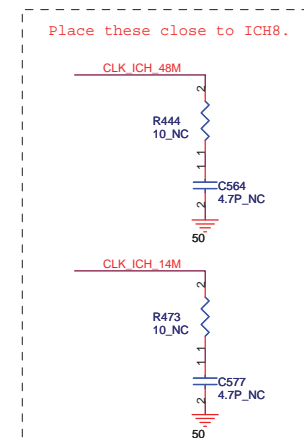
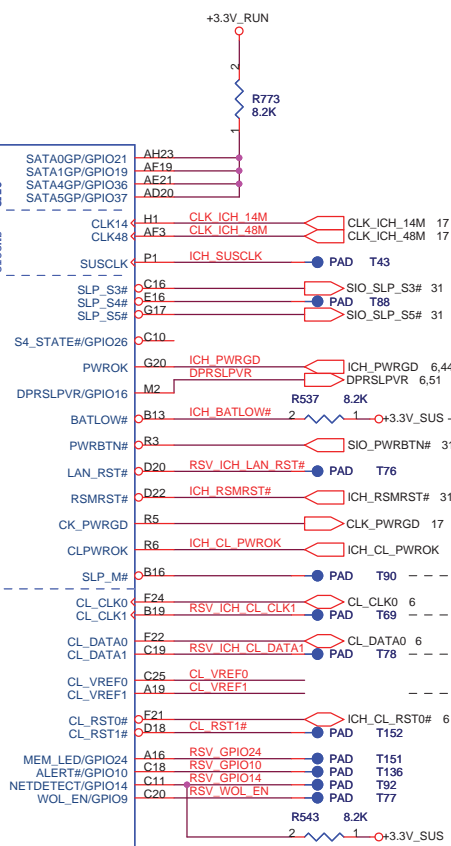
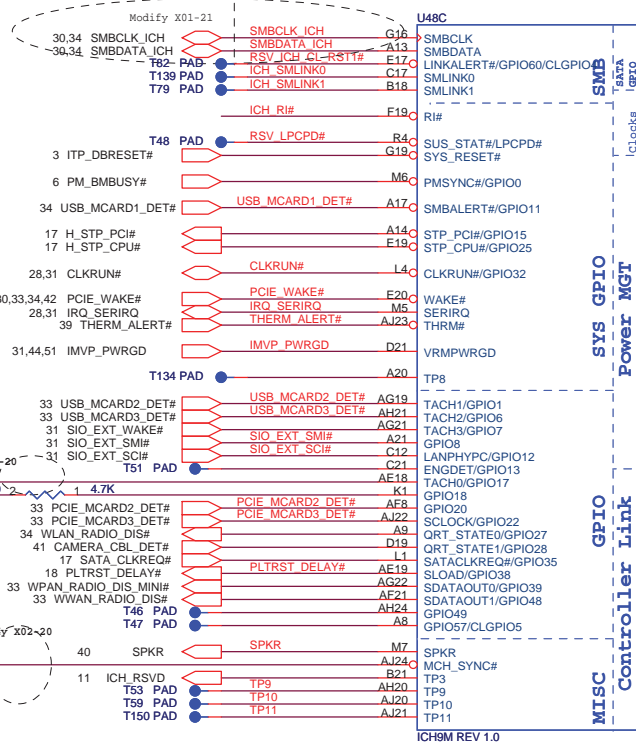
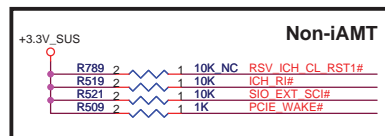
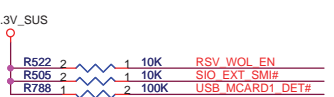
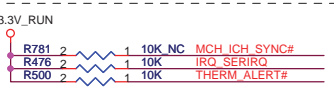
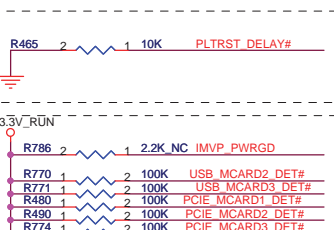
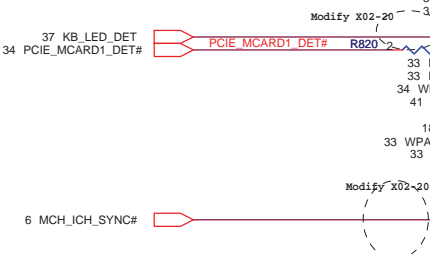
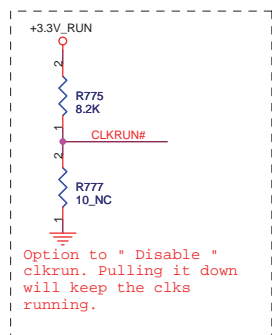


		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Places within 500 mils of the ICH9

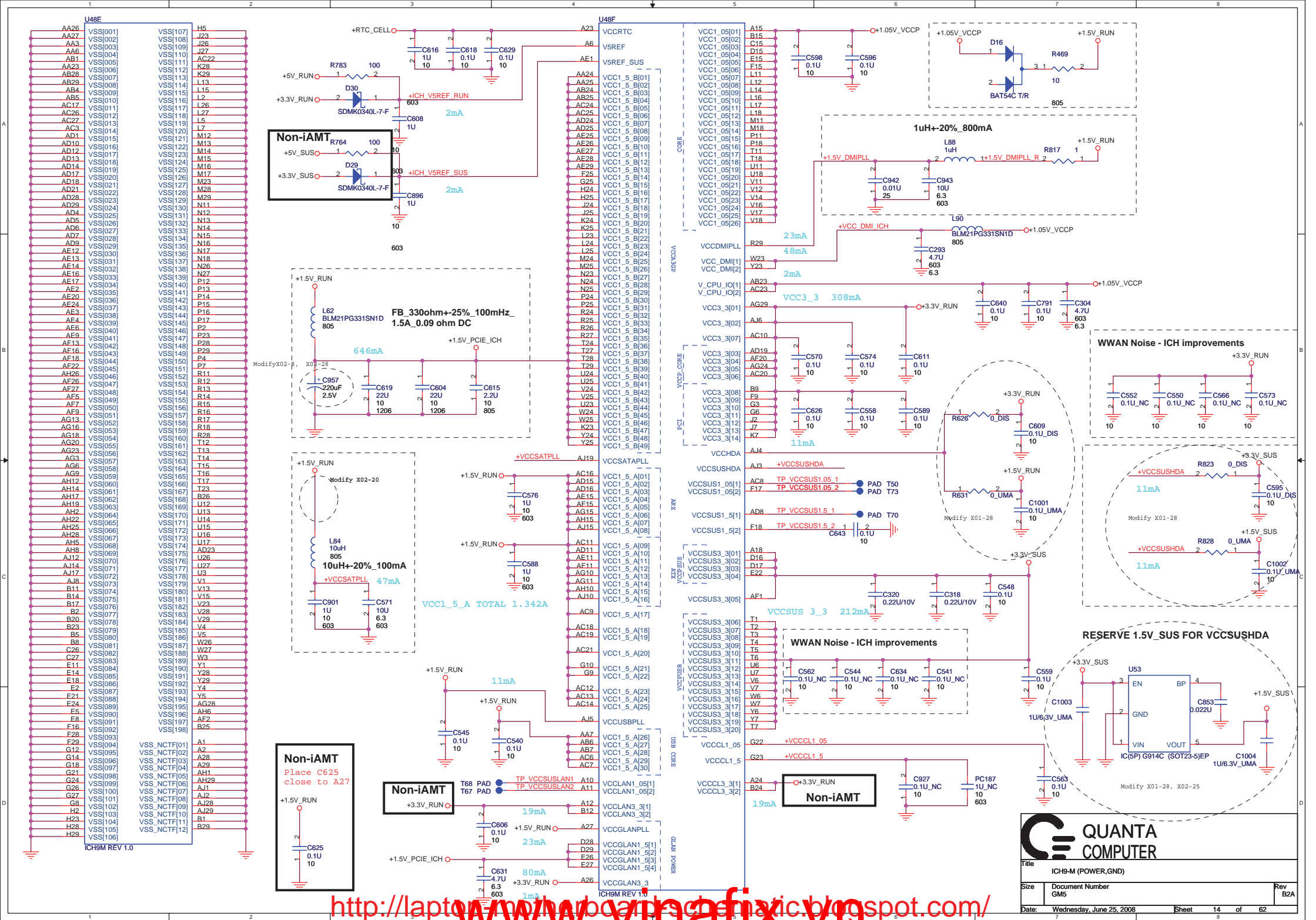
WWAN Noise - ICH improvements



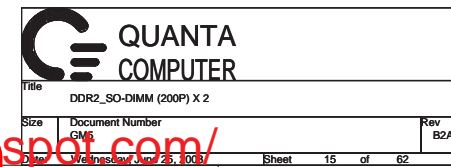


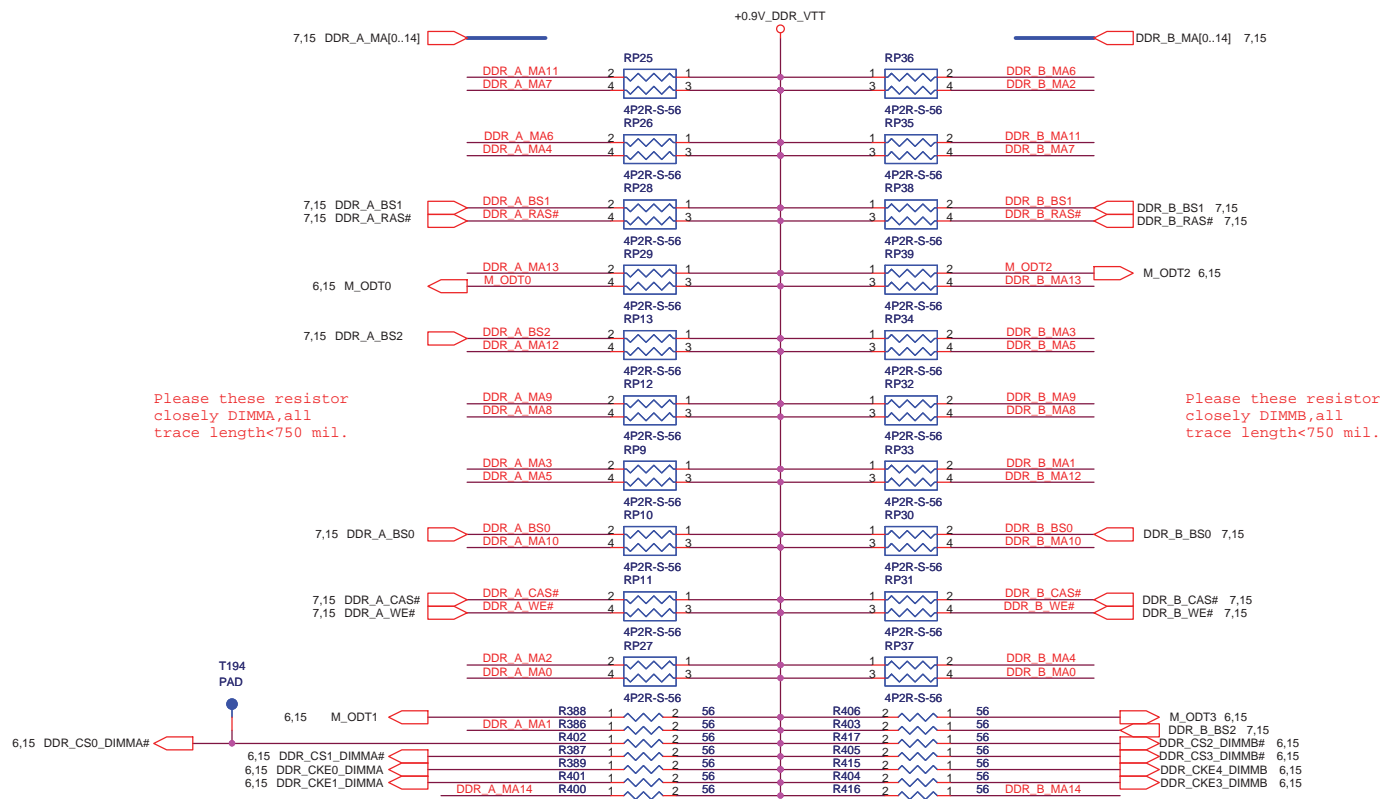
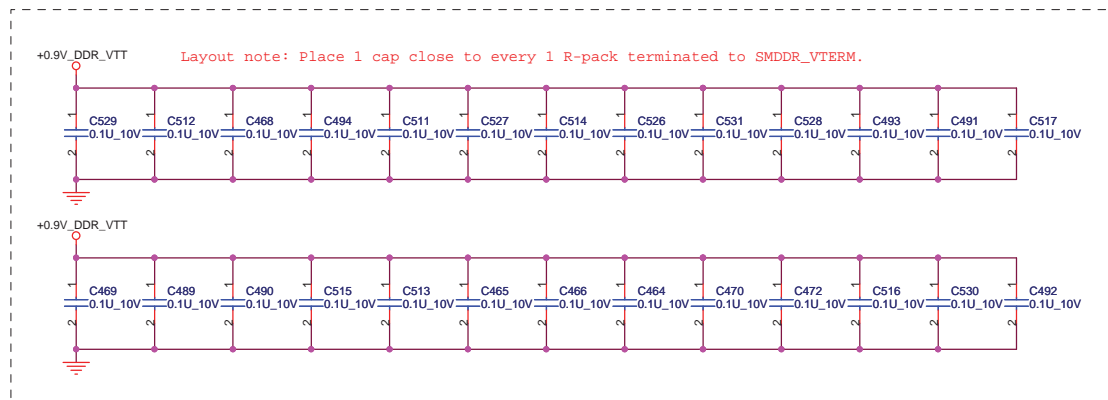
Non-iAMT

A circuit diagram showing a connection between two pins. A red line from a pin labeled "3.3V_RUN" goes down to a resistor symbol labeled "R478" and "1K_NC". From the bottom of the resistor, a red line goes down to a pin labeled "SPKR".

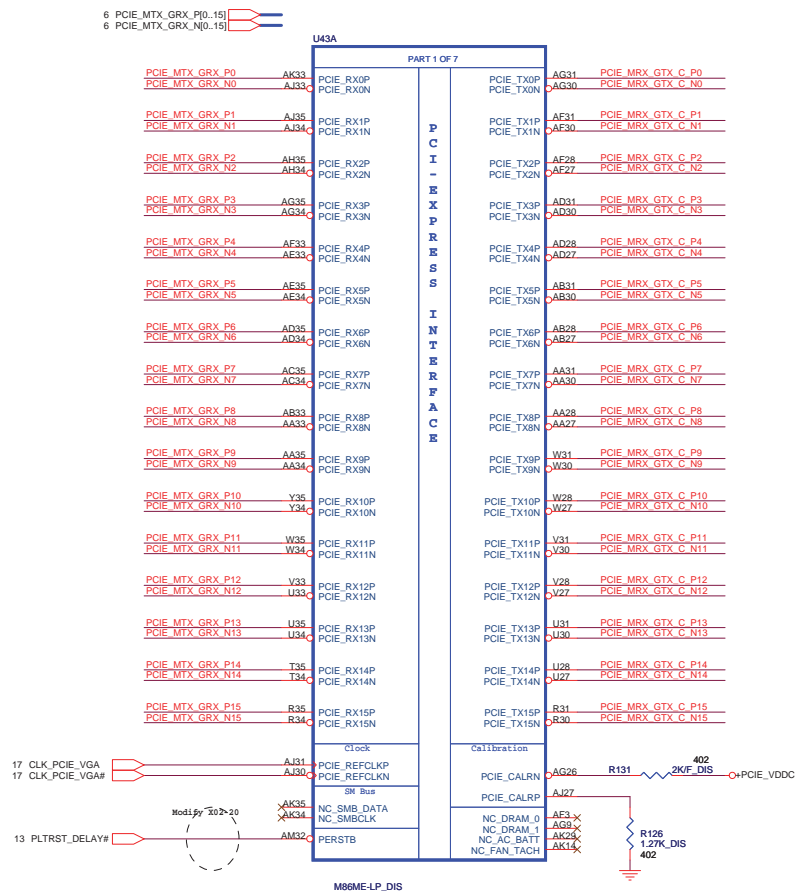


SLAVE





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DDR2 RES. ARRAY		
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Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
400 MHz 256MB(16M*16) Hynix	1	1	1	1
400 MHz 256MB(16M*16) Qimonda	1	1	1	0
500 MHz 256MB(16M*16) Hynix	1	1	0	1
500 MHz 256MB(16M*16) Qimonda	1	1	0	0
500 MHz 256MB(16M*16) Samsung	1	0	1	1

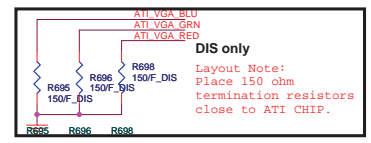
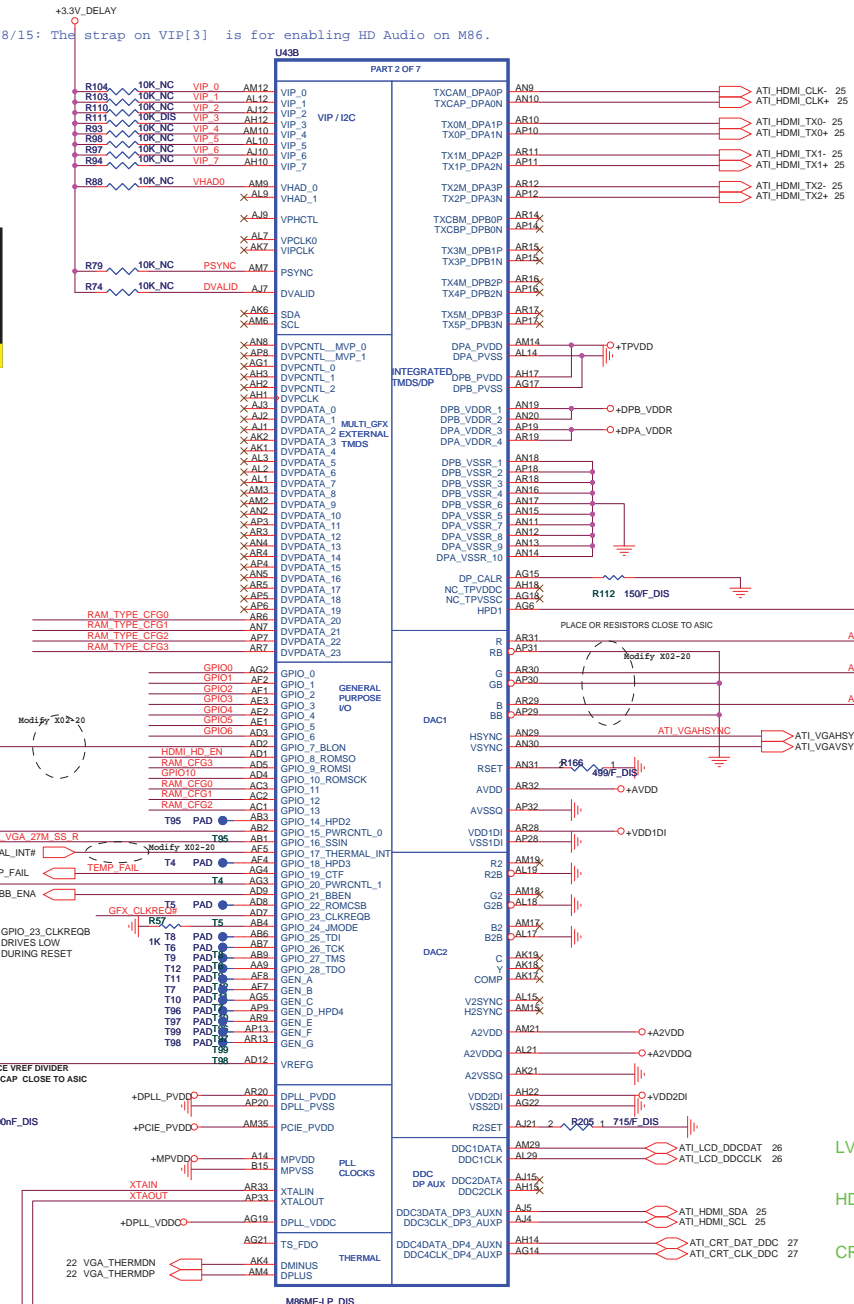
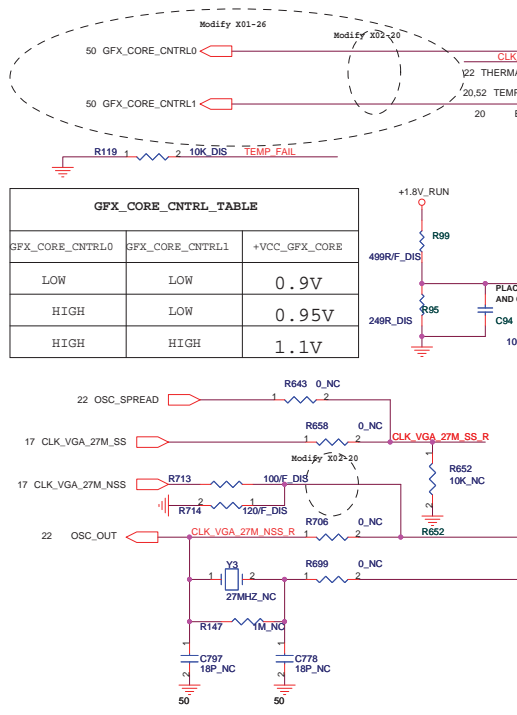
The diagram shows the pinout of the RAM module. The top section is labeled +3.3V_DELAY and includes pins R644 (10K_DIS RAM_CFG0), R648 (10K_NC RAM_CFG1), R650 (10K_NC RAM_CFG2), and R654 (10K_NC RAM_CFG3). The bottom section is labeled +1.8V_RUN and includes pins R667 (10K_DIS RAM_TYPE_CFG0), R668 (10K_DIS RAM_TYPE_CFG1), R669 (10K_NC RAM_TYPE_CFG2), and R674 (10K_DIS RAM_TYPE_CFG3). The text 'VRAM SIZE' and 'VRAM TYPE' are placed to the right of their respective pin groups.

4.3.3V_DELAY

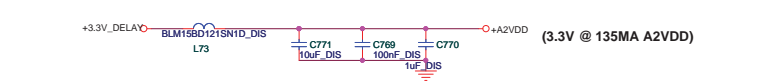
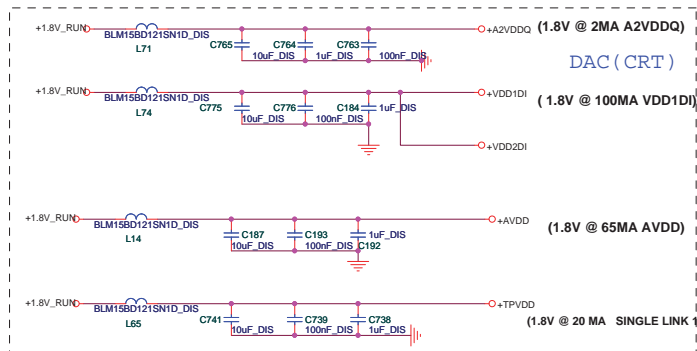
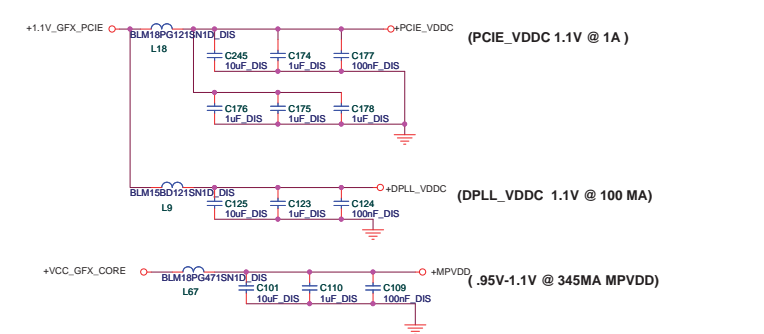
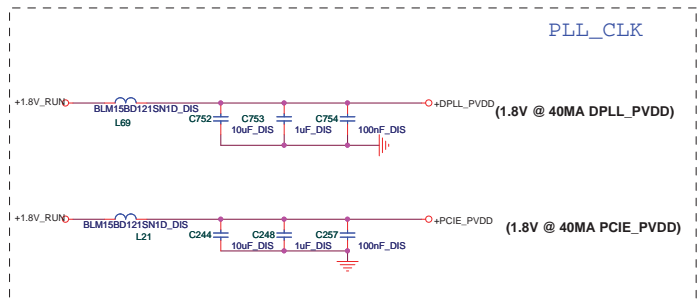
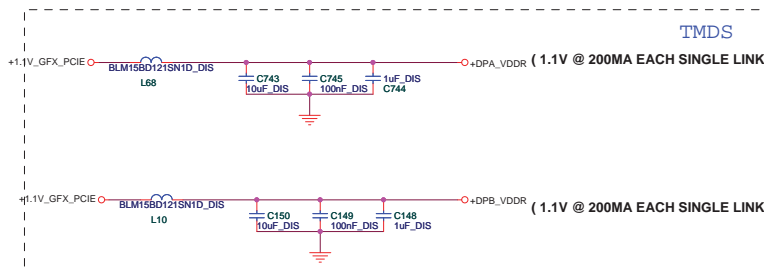
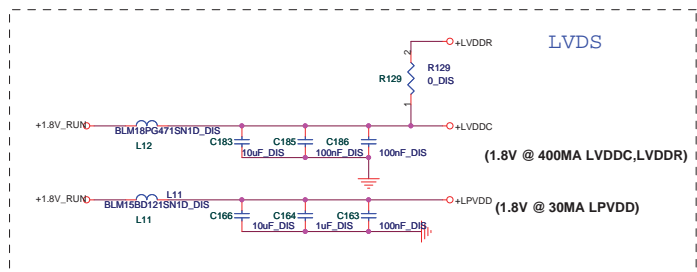
R651	10K	GPIO0
R650	10K NC	GPIO1
R652	10K NC	GPIO2
R653	10K NC	GPIO3
R645	10K NC	GPIO4
R656	10K NC	GPIO5
R646	10K NC	GPIO6
R649	10K NC	HDMI HD_EN
R65	10K NC	GPIO10
R148	10K DIS	ATI VGAHSYNC
R61	10K NC	GPIO CLKREQ#
R666	10K NC	TEMP_FAULT

31 ATI_PANEL_BKEN

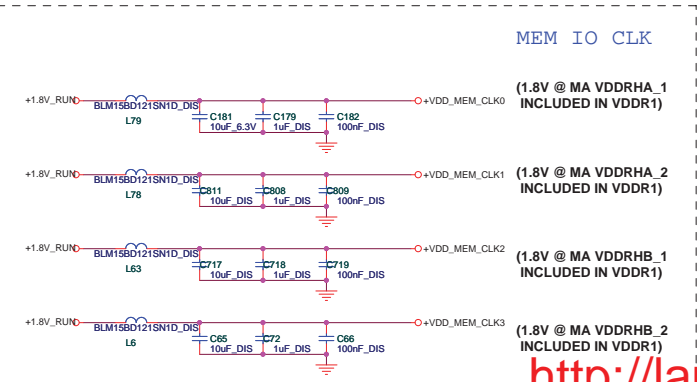
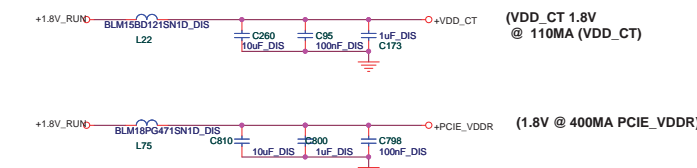
GFX_CORE_CNTRL_TABLE		
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.1V







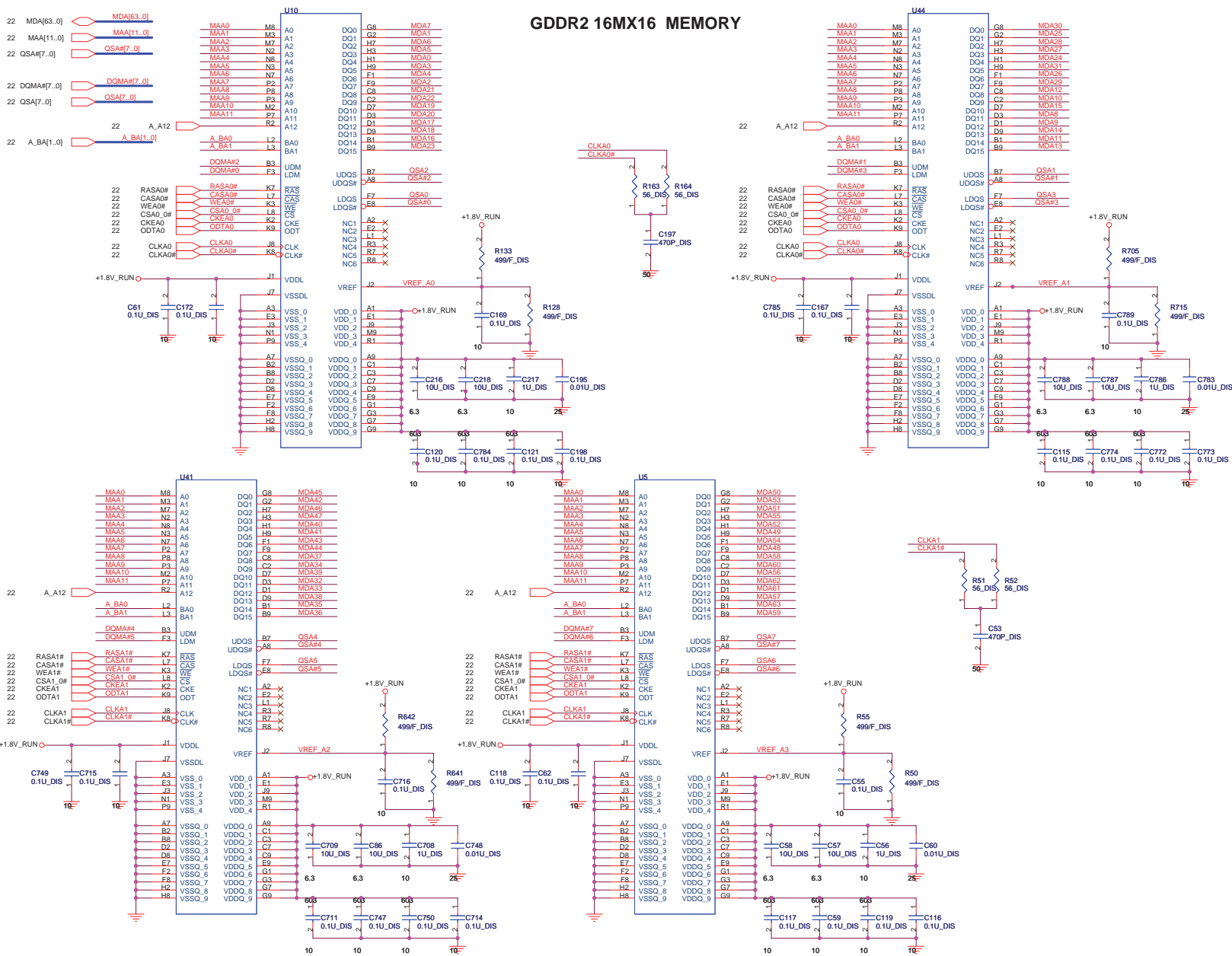
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



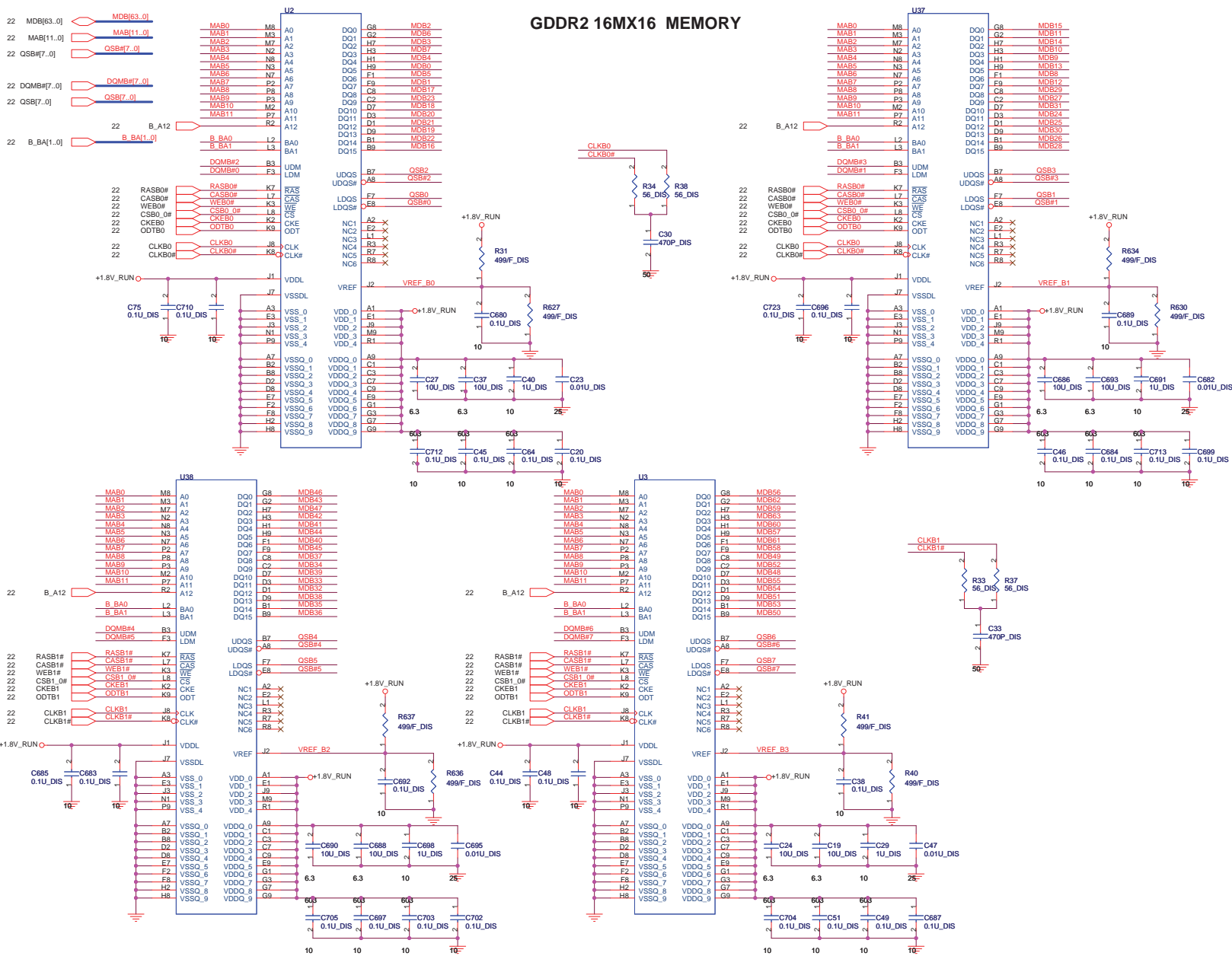
<http://laptop-motherboardschematic.blogspot.com/>

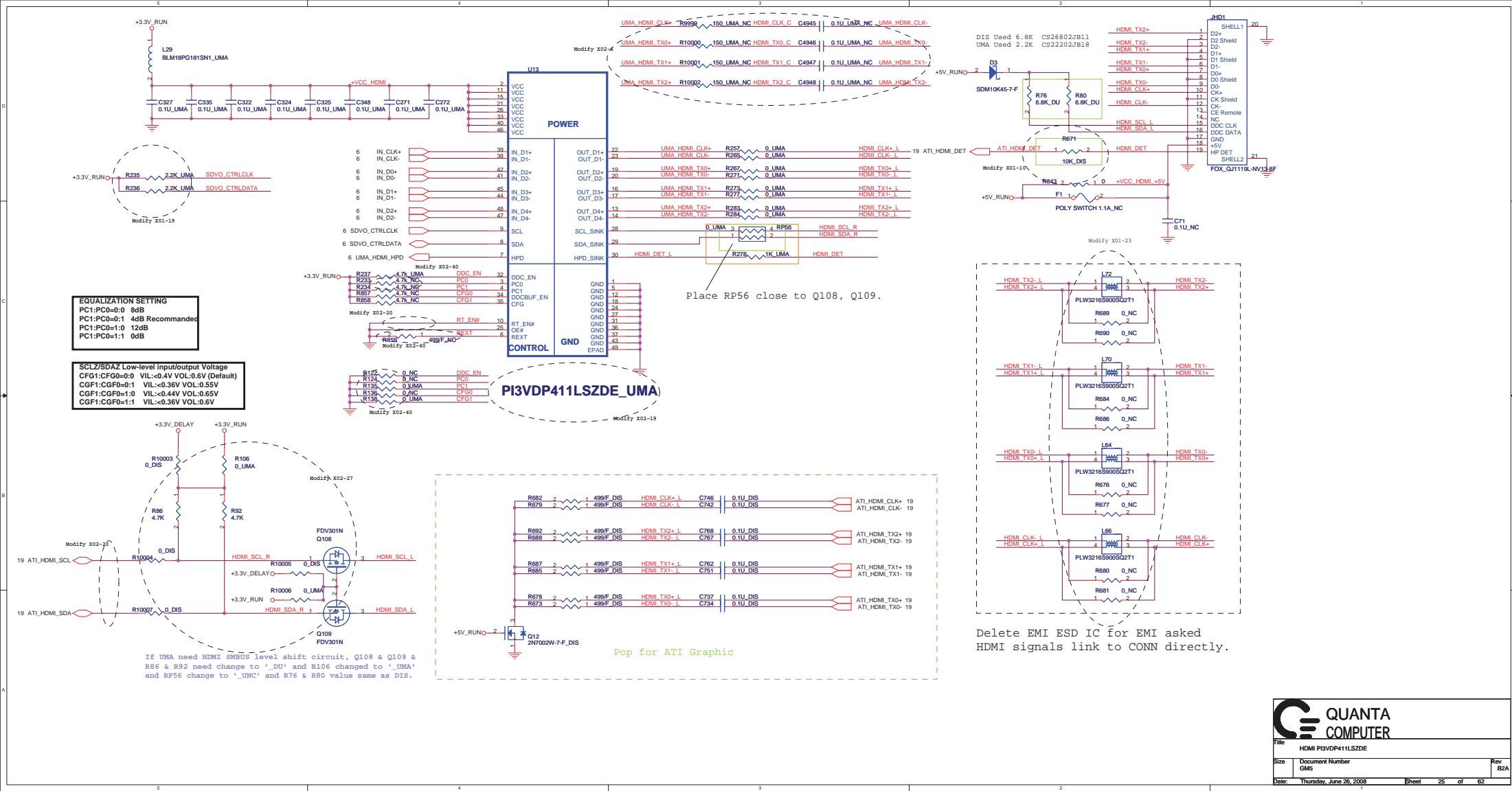
www.vinafix.vn

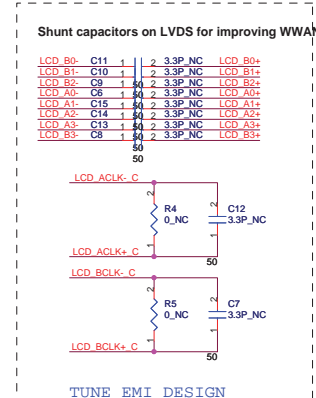
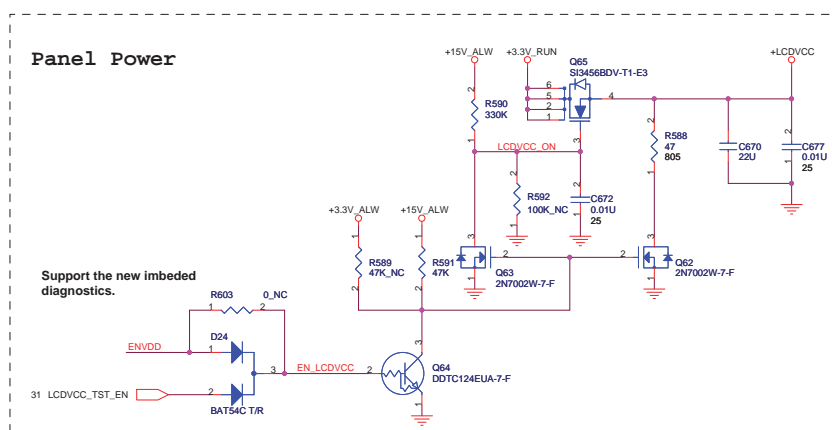
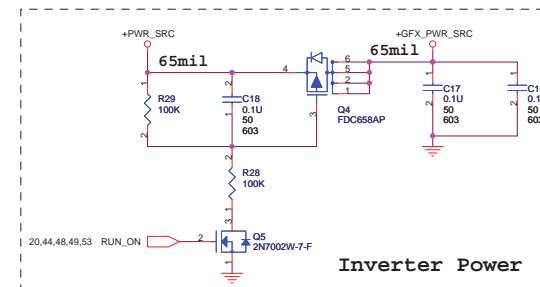
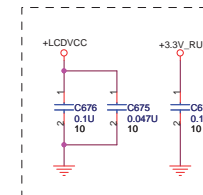
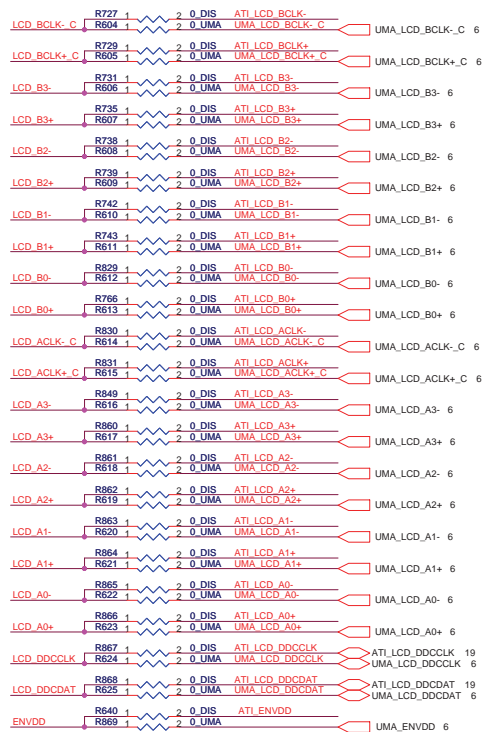
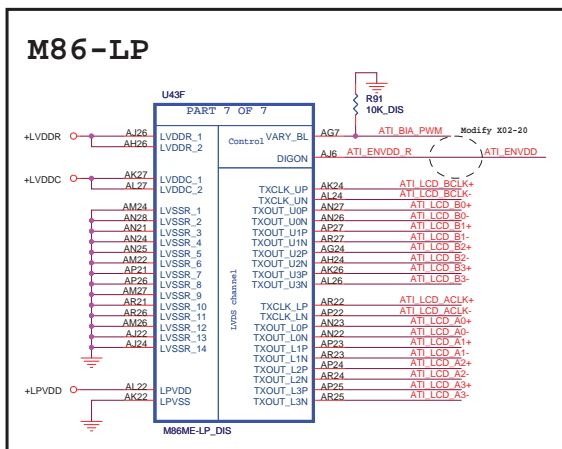
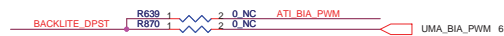
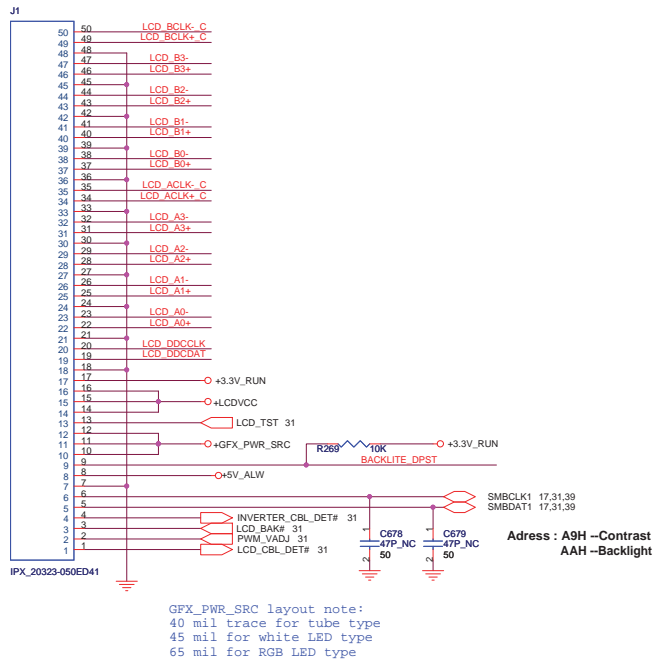
GDDR2 16MX16 MEMORY

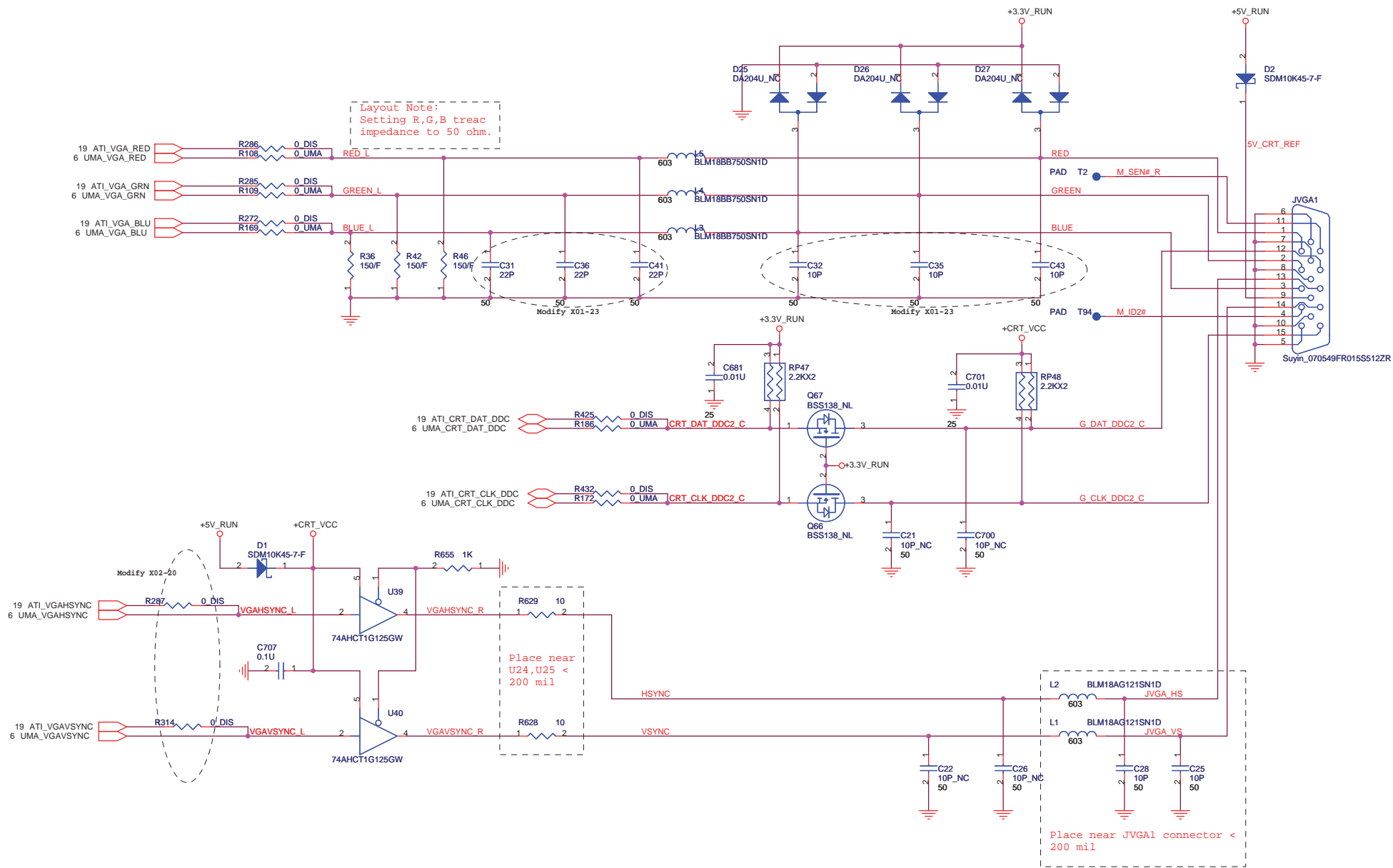


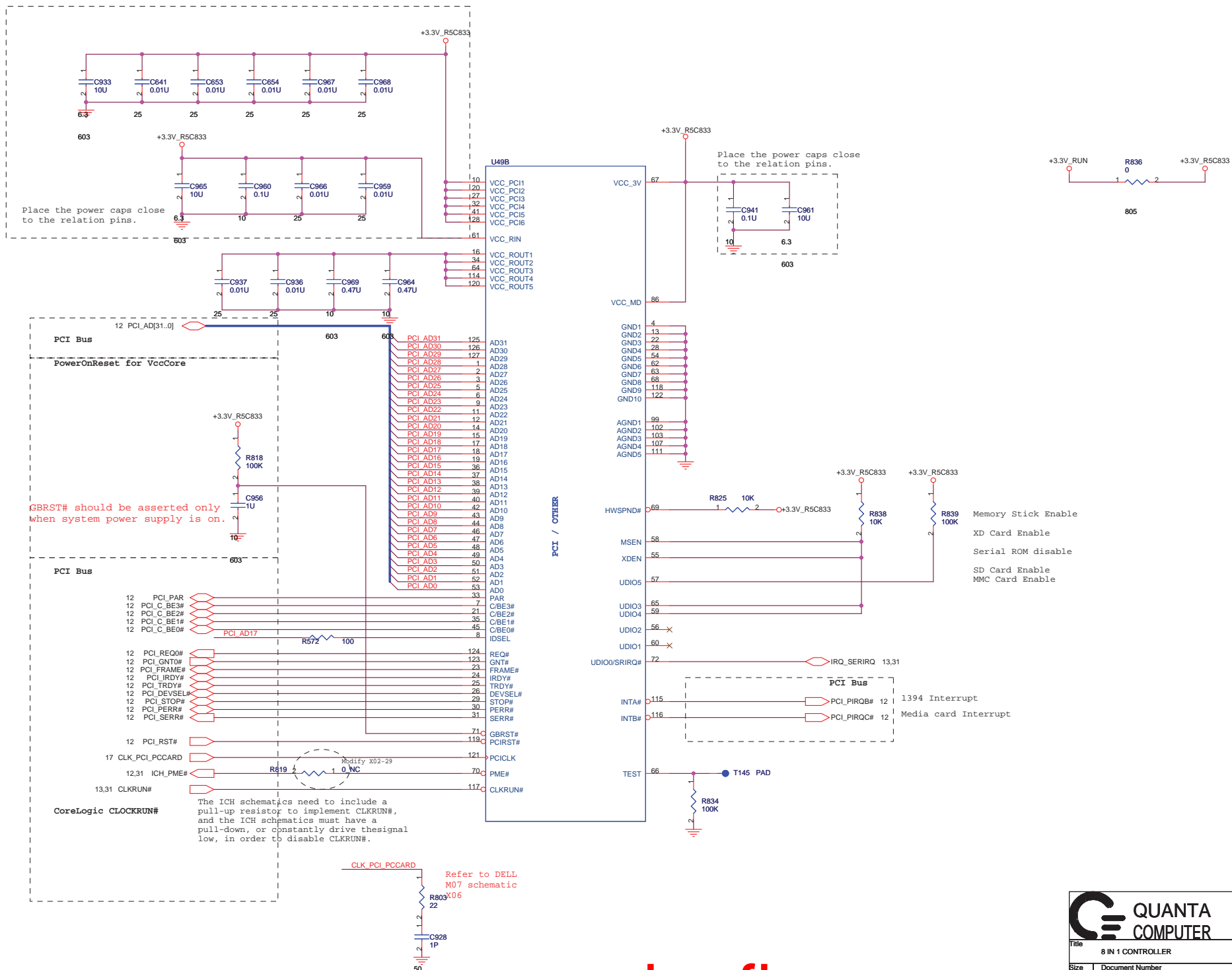
GDDR2 16MX16 MEMORY

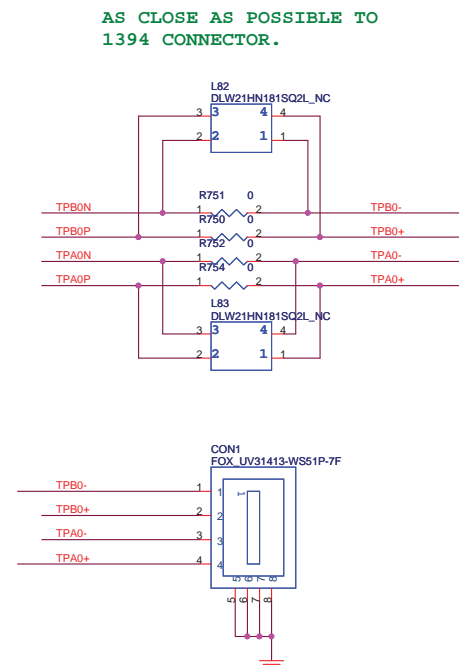












Please the cap
near connector.

+3.3V_CARD

C579 0.1u

C582 0.1u

C572 10u

10 10 6.3

Please place cap near connector.

603

Modify X01-21

13,34 SMBCLK_I

13,34 SMBDATA_I

+1.5V_CARD

+3.3V_CARD

17 CARD_CLK_REQ

31 EXPRCDR_PWREN#

17 CLK_PCIE_EXP_CARD

17 CLK_PCIE_EXP_CARD

12 PCIE_RX4

12 PCIE_RX4+

12 PCIE_TX4

12 PCIE_TX4+

CON2

GND_1

USB1

USB2

USB3

CPUSB#

RSV_0

RSV_1

SMBCLK

SMBDATA

+1.5V_0

+1.5V_1

WAKE#

+3.3VAUX

PERST#

+3.3V_1

+3.3V_2

CLKREQ#

CPE#

REFCLK-

REFCLK+

GND_2

PERn0

PERn0

GND_3

PETn0

PETp0

GND_4

NC1

NC2

NC3

















NC4

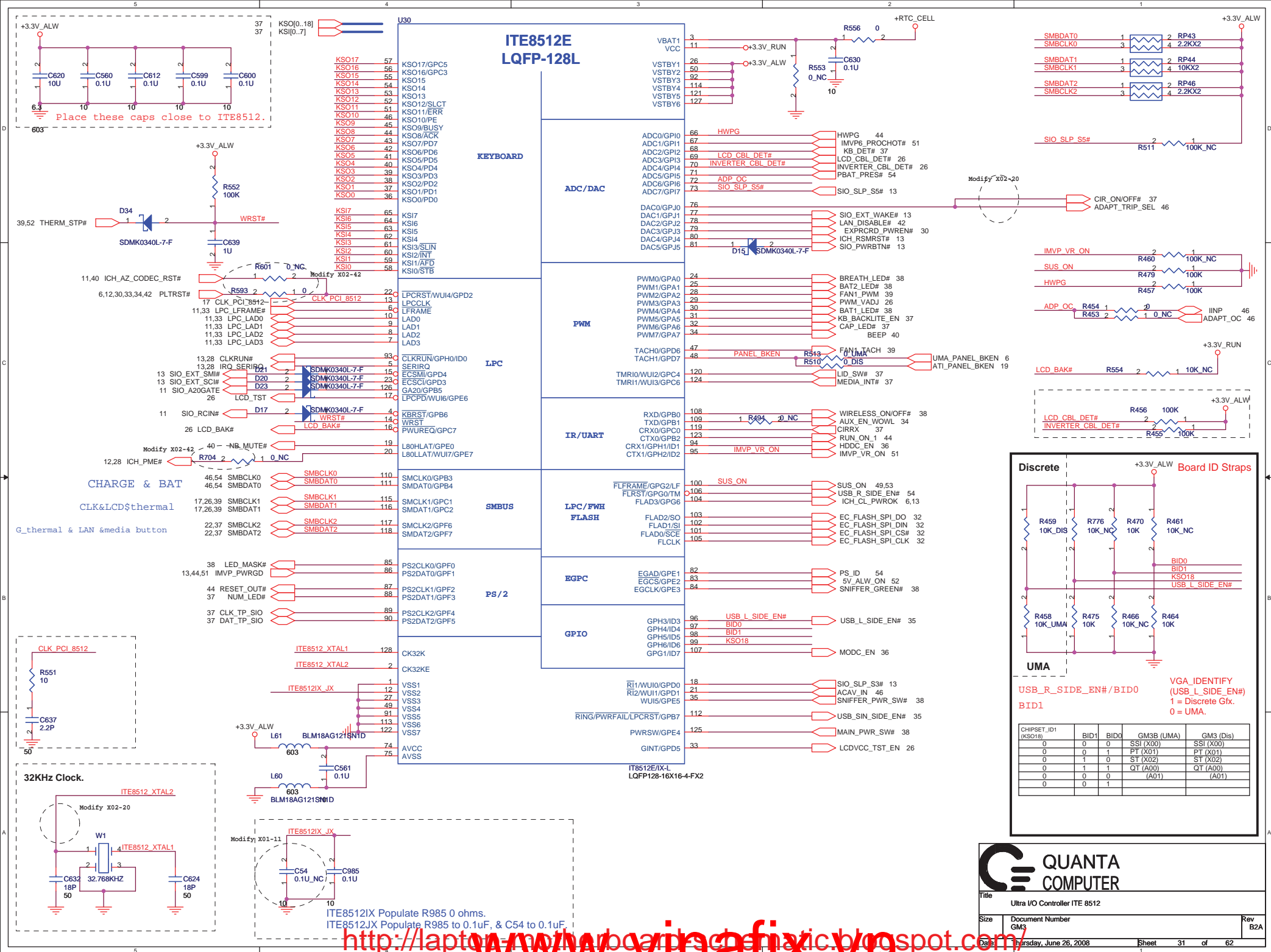
FOX_1CH41BAC-GM

JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector.

[illegible][illegible]

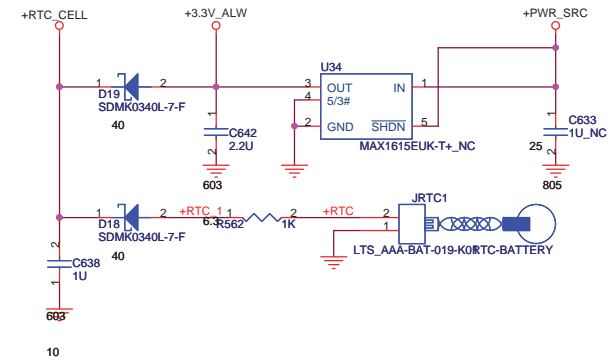
29	XD_CDSW#	
29	SD_WP#(XDR/B#)	
29	XD/MMC_DATA7	
29	XD/MMC_DATA6	
29	XD/MMC_DATA5	
29	XD/MMC_DATA4	
29	SD/XDMS_DATA3	
29	SD/XDMS_DATA2	
29	SD/XDMS_DATA1	
29	SD/XDMS_DATA0	
29	SD/XDMS_CMD	
29	XD_WP#	
29	XD_ALE	
29	XD_CLE	
29	XD_CE#	
29	SD/XDMS_CLK	



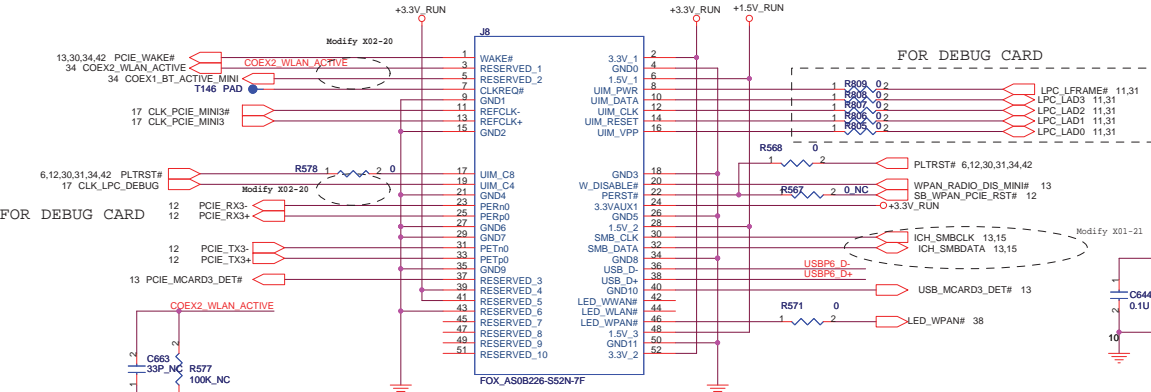
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31 EC_FLASH_SPI_CS#
31 EC_FLASH_SPI_CLK
31 EC_FLASH_SPI_DIN
31 EC_FLASH_SPI_DO
```



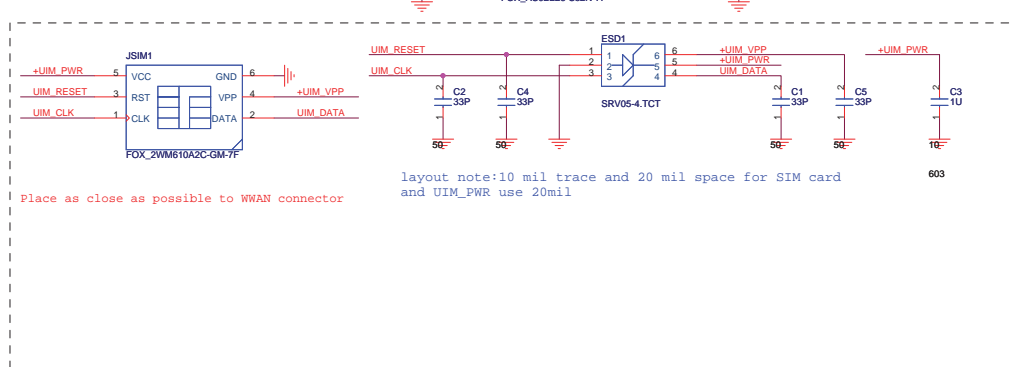
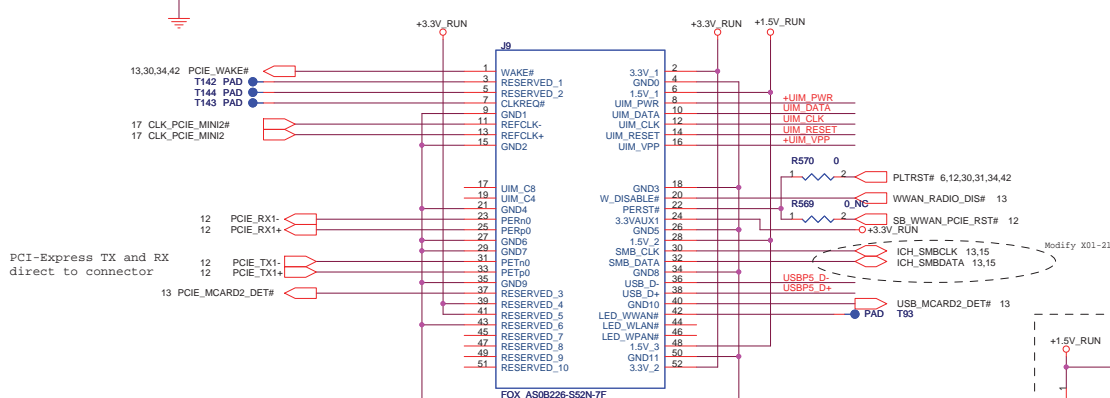
RTC BATTERY



MiniCard Robson, UWB connector

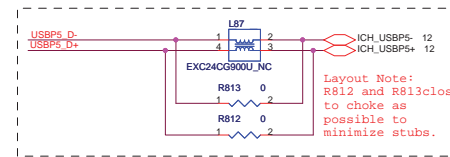
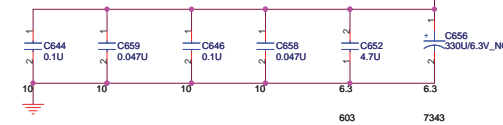
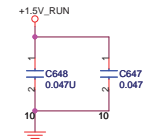
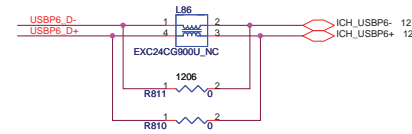


MiniCard WWAN connector

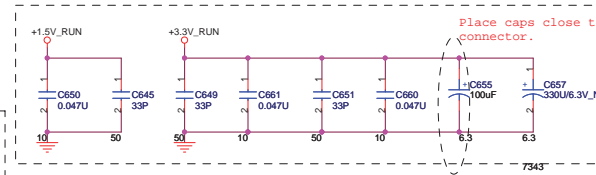


layout note: 10 mil trace and 20 mil space for SIM card and UIM_PWR use 20mil

Place as close as possible to WWAN connector



Layout Note: R812 and R813 close to choke as possible to minimize stubs.



Modify X01-21



WWAN, WPAN

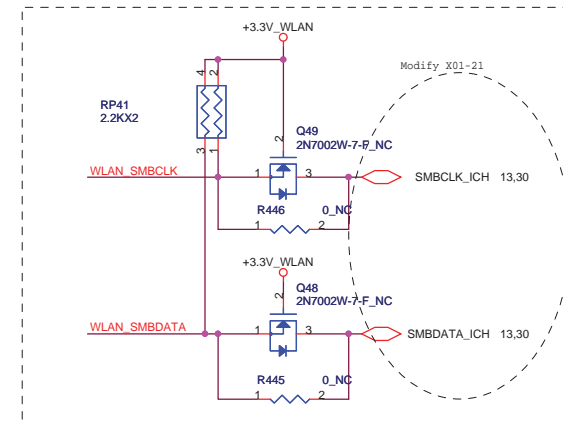
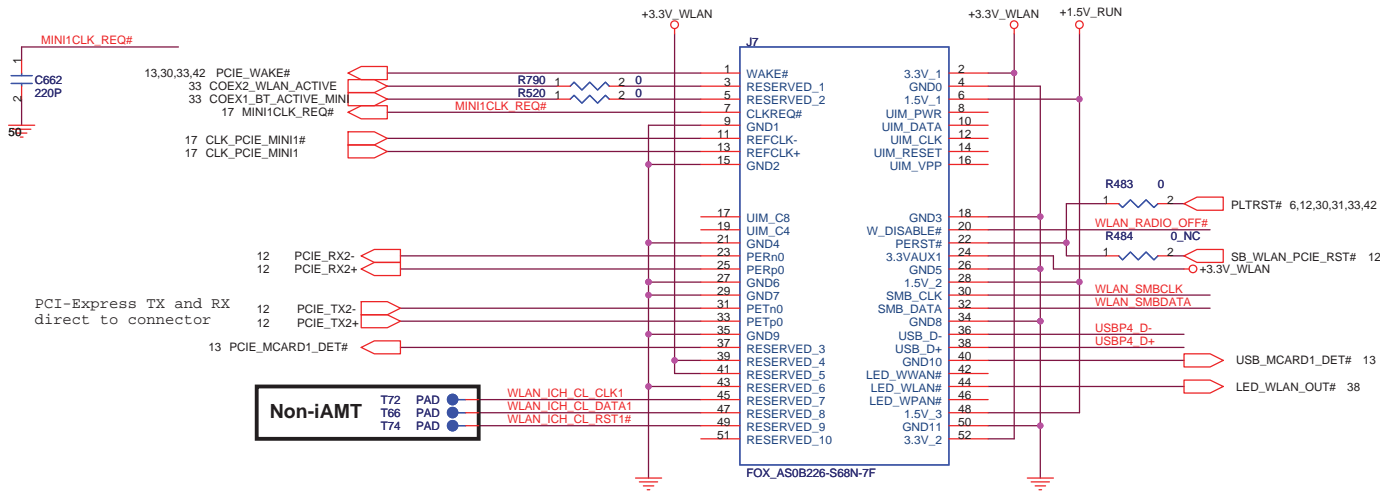
WLAN, WPAN

WLAN, WPAN

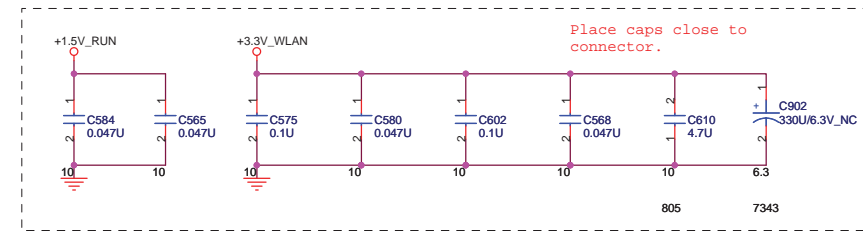
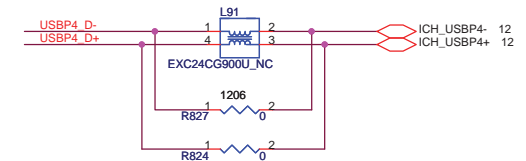
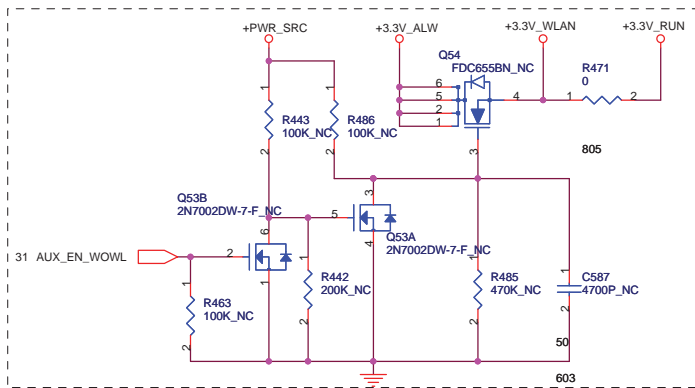
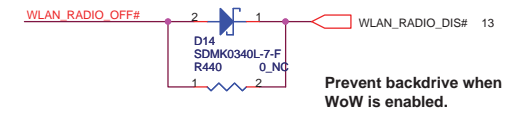
WLAN, WPAN

WLAN, WPAN

MiniCard WLAN connector



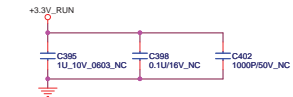
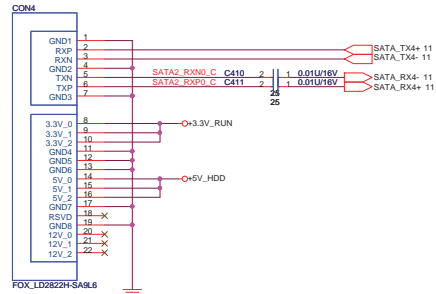
Support for WoW



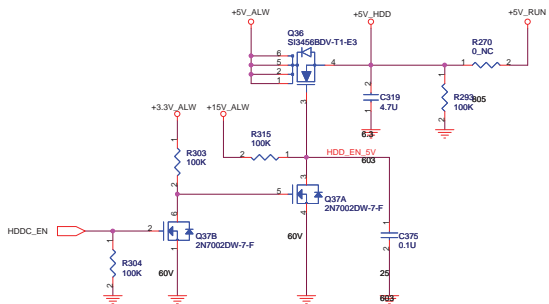
Title WLAN		
Size	Document Number GMS	Rev B2A
Date	Wednesday, June 25, 2008	Sheet 34 of 62

SATA Connector.

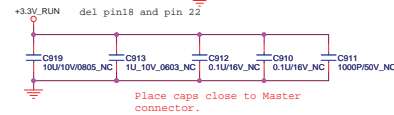
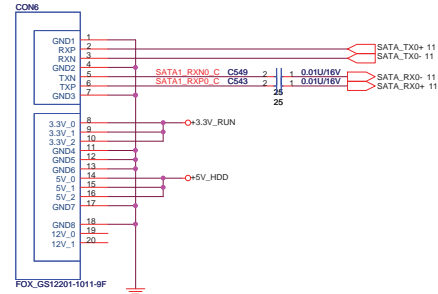
Second HDD



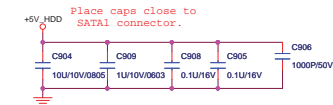
Place caps close to Second HDD connector.



Master

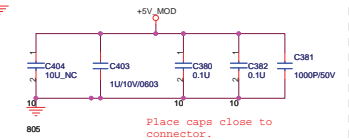
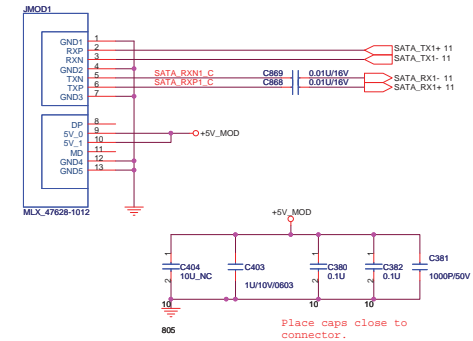


Place caps close to Master connector.

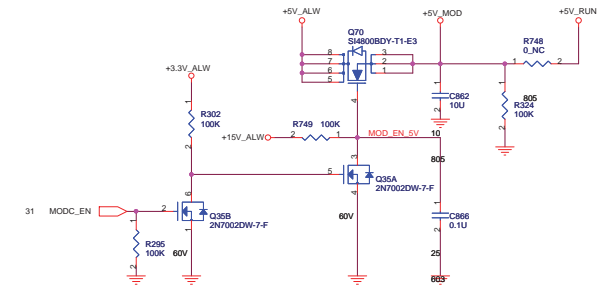


Place caps close to SATA1 connector.

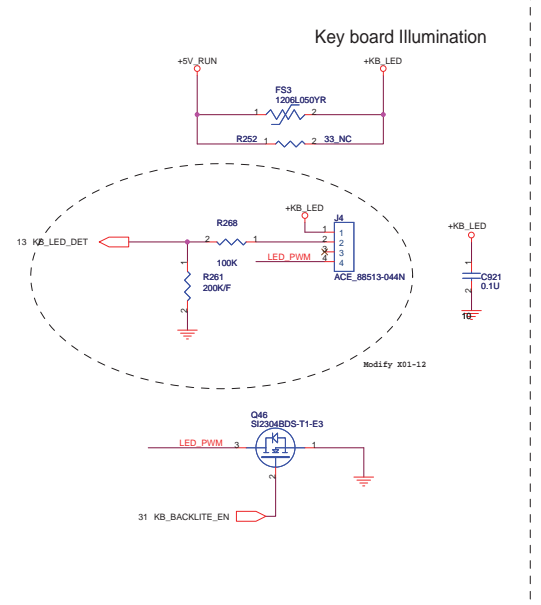
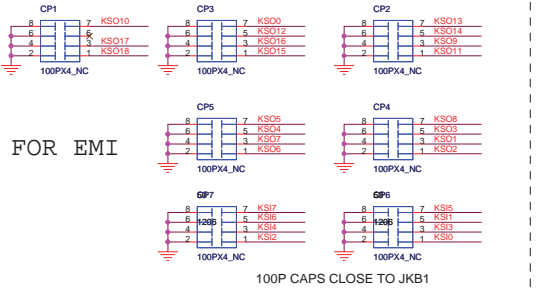
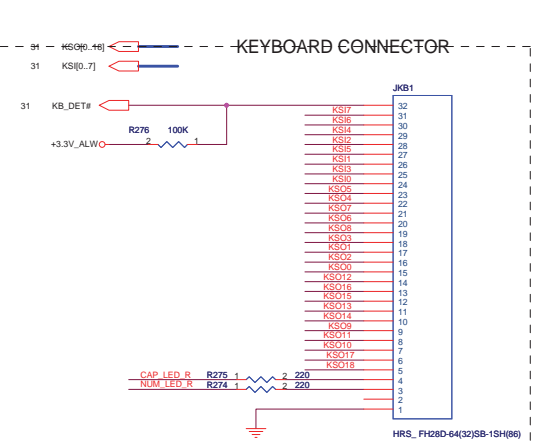
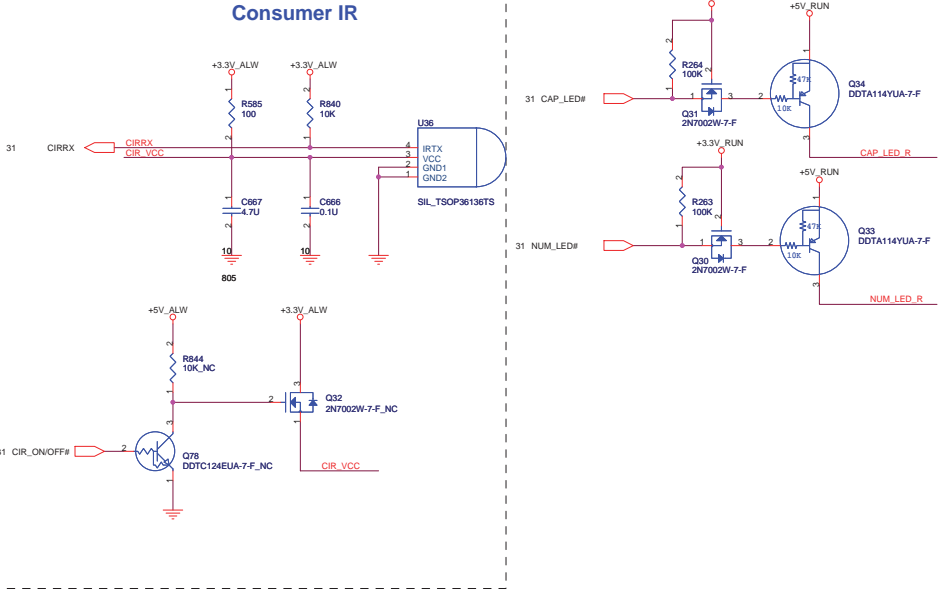
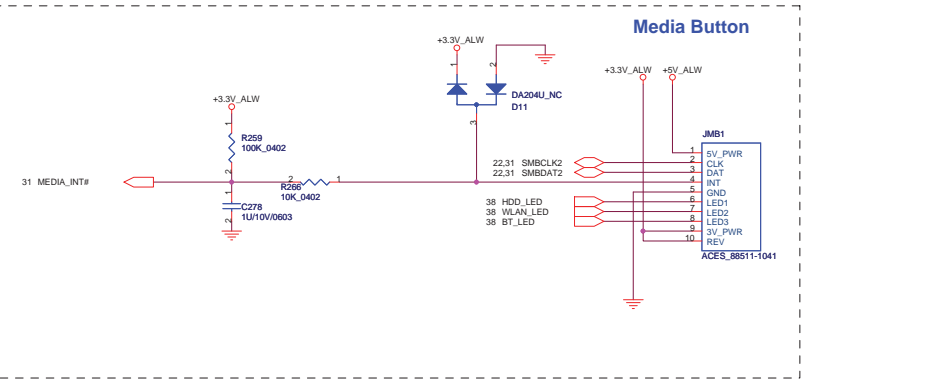
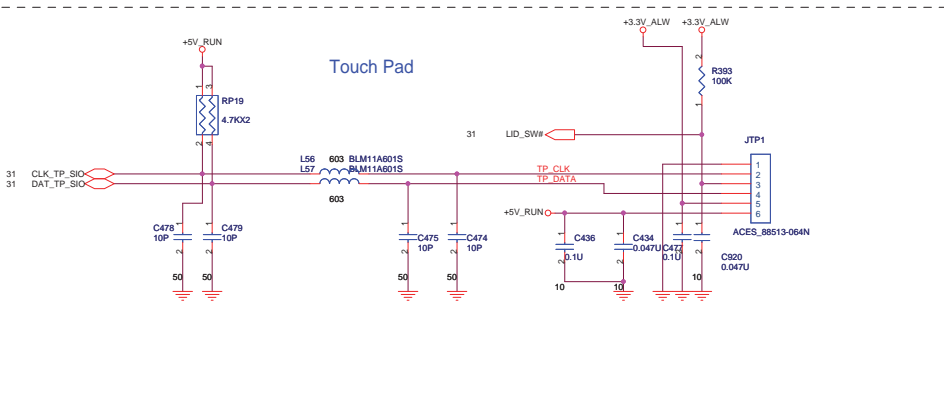
ODD Connector



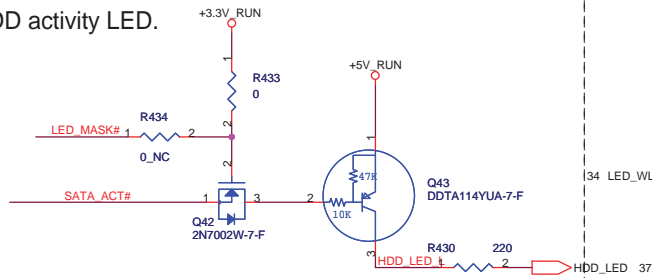
Place caps close to connector.



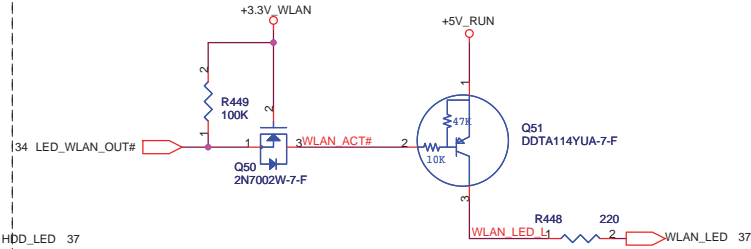
File	SATA (HDD&CD_ROM)	Rev	B2A
Size	Document Number		
	GMS		
Date	Wednesday, June 25, 2008	Sheet	38 of 62



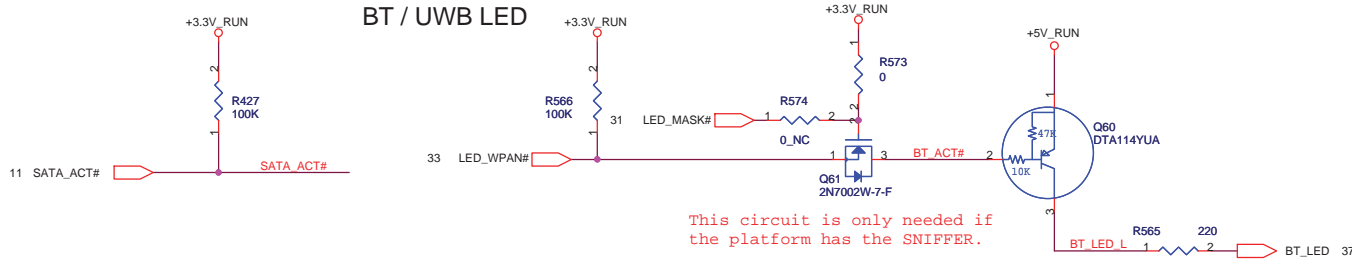
HDD activity LED.



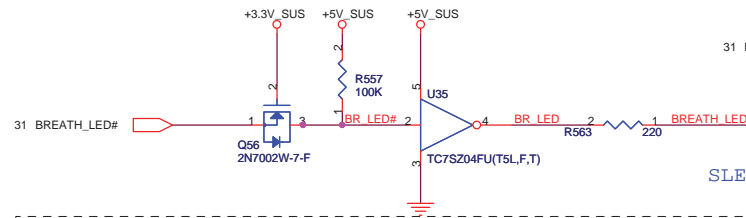
WLAN



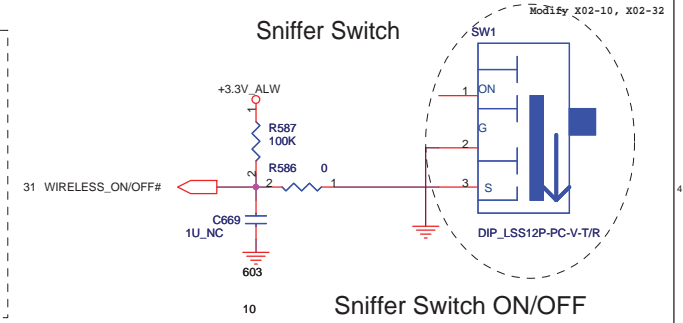
BT / UWB LED



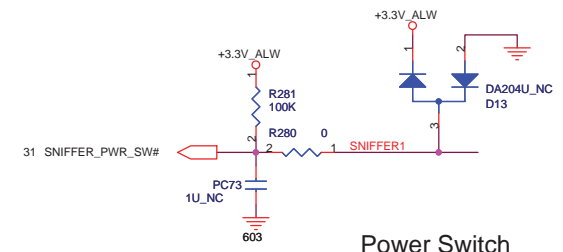
Power & Suspend.



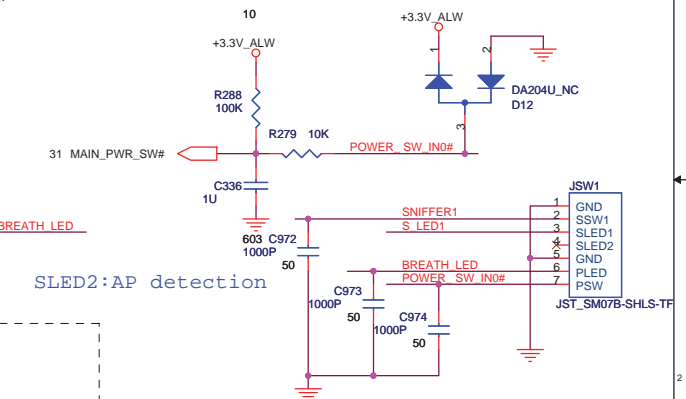
Sniffer Switch



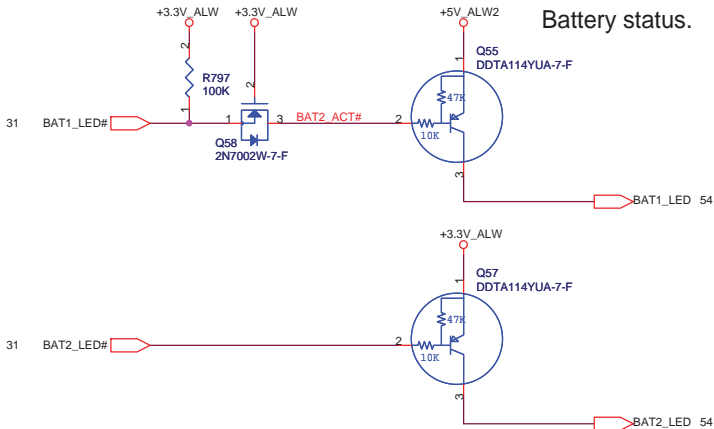
Sniffer Switch ON/OFF



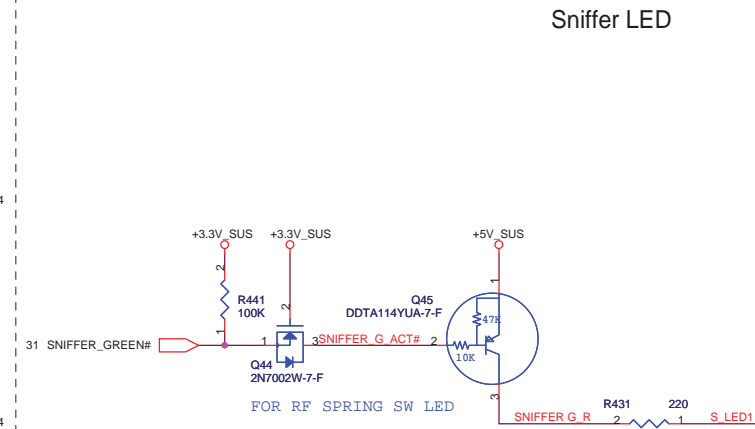
Power Switch



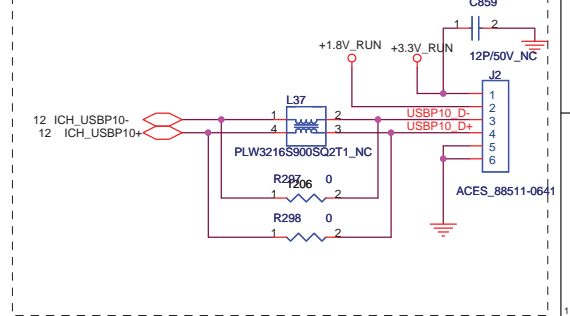
Battery status.



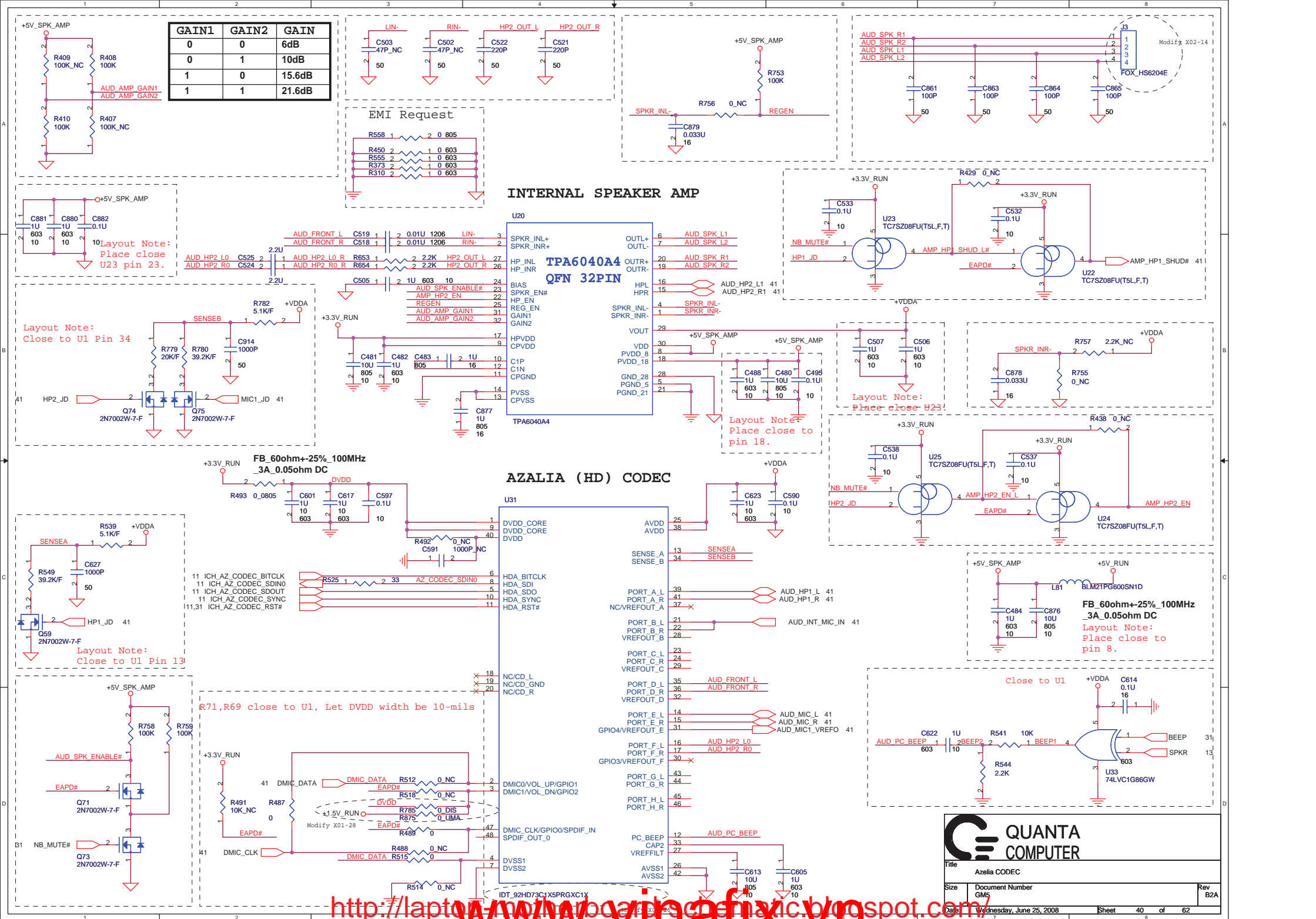
Sniffer LED



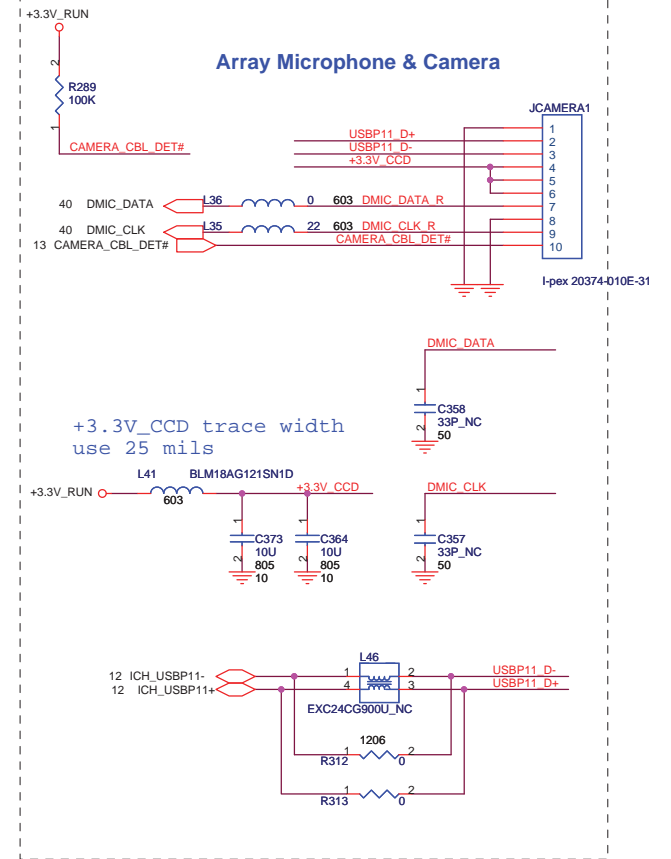
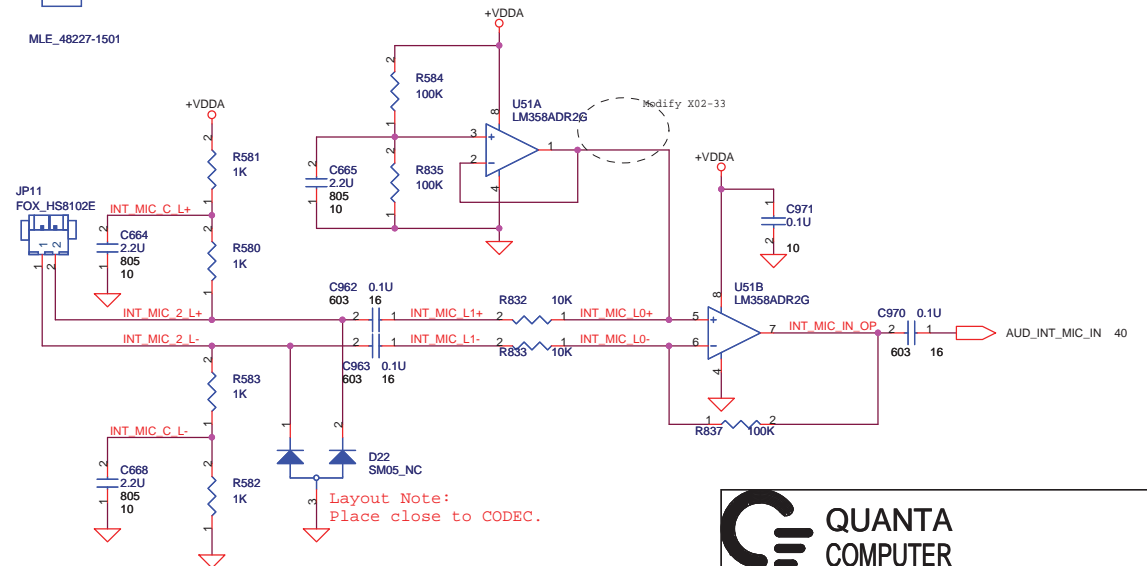
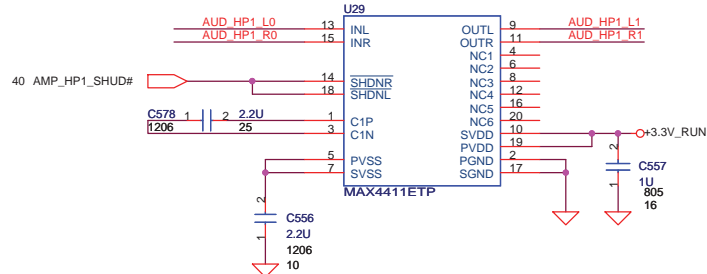
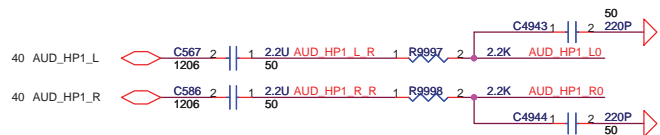
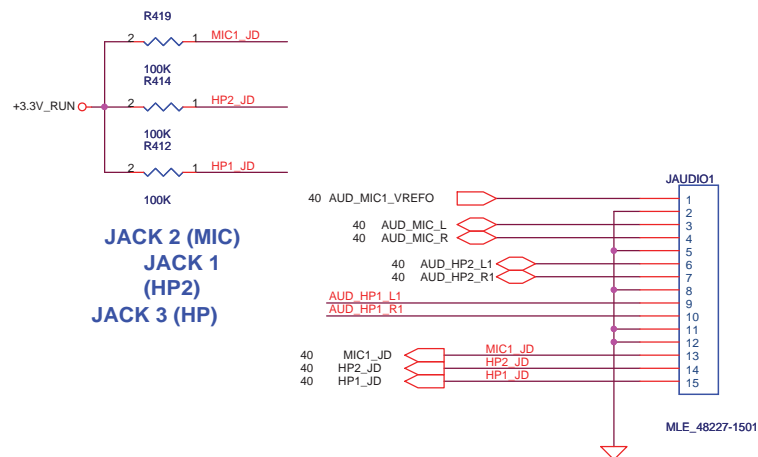
Biometric



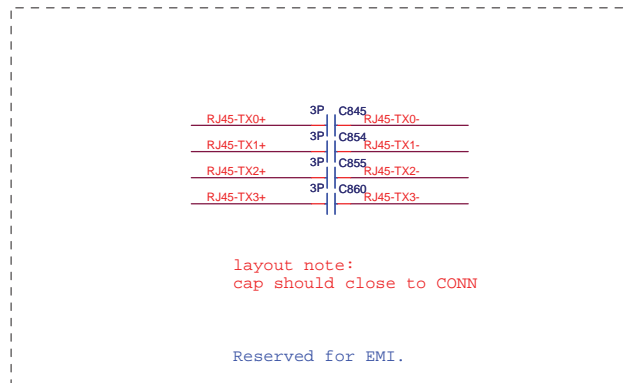
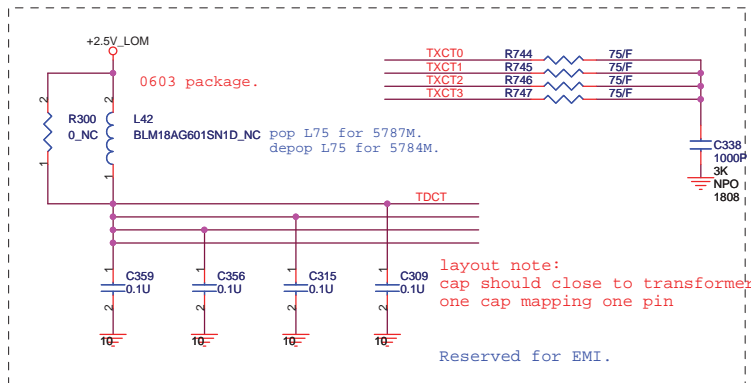
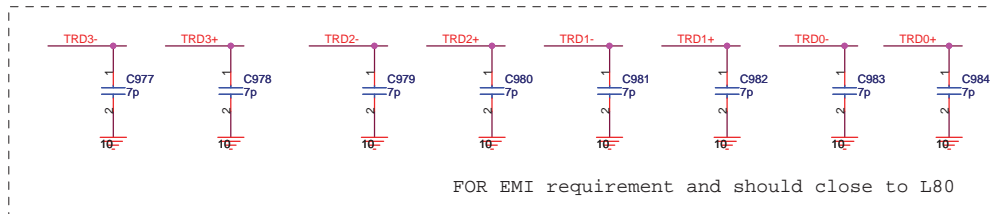
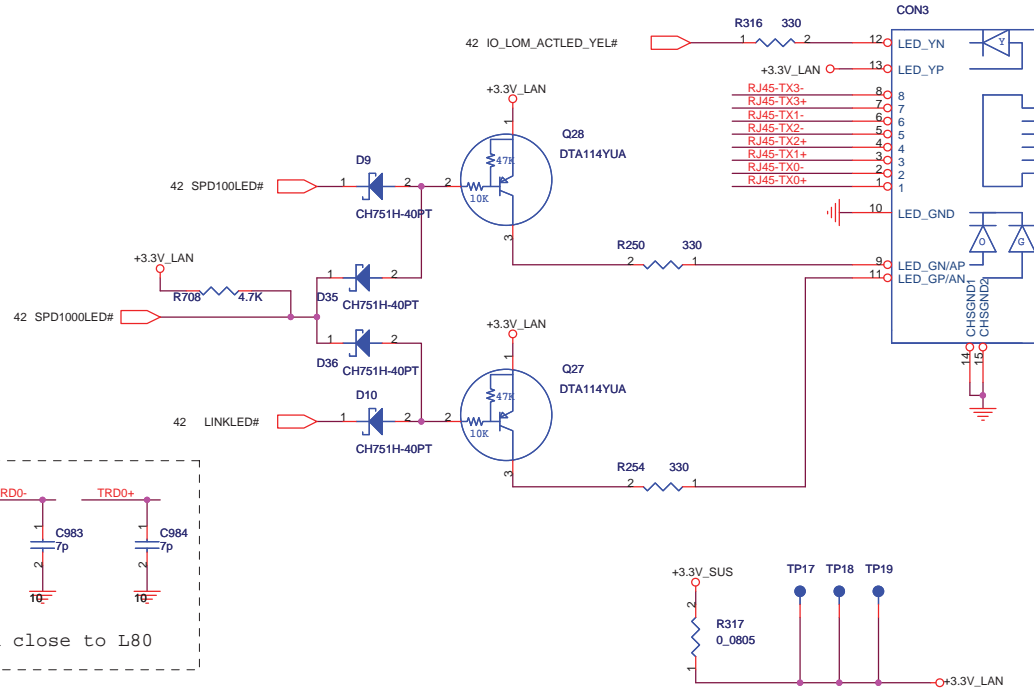
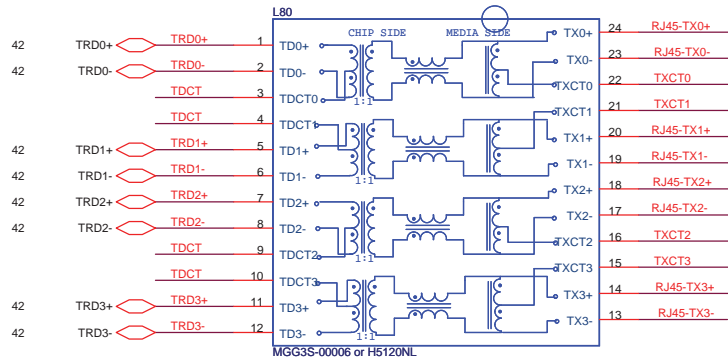
Title			SWITCH, KEYBOARD & LED		
Size	Document Number	Rev		B2A	
GM5					
Date	Wednesday, June 25, 2008	Sheet	38	of	62



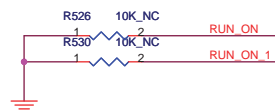
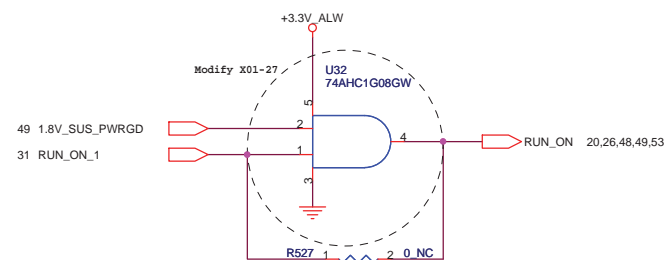
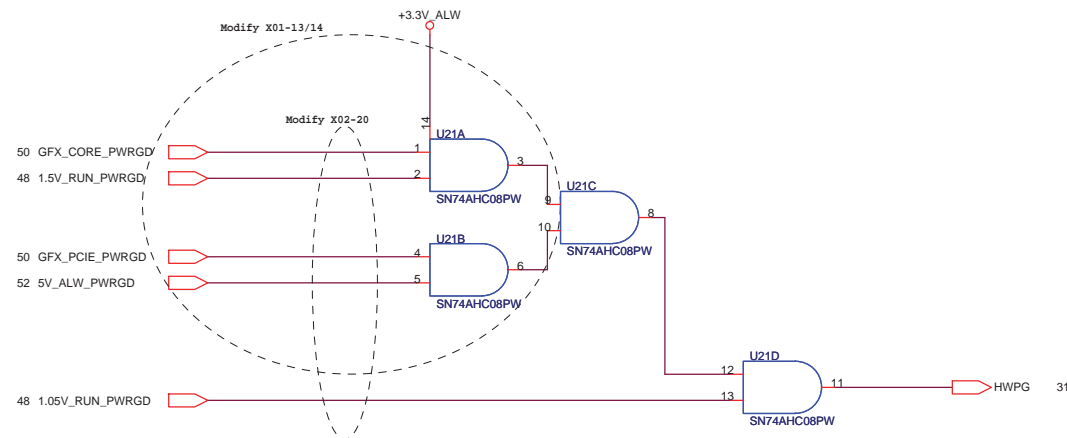
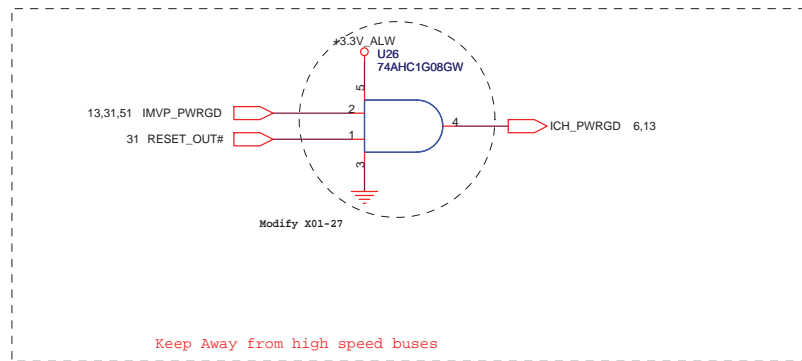
Headphone Jack Stereo MIC Jack




TRANSFORM




RJ-45 Connector

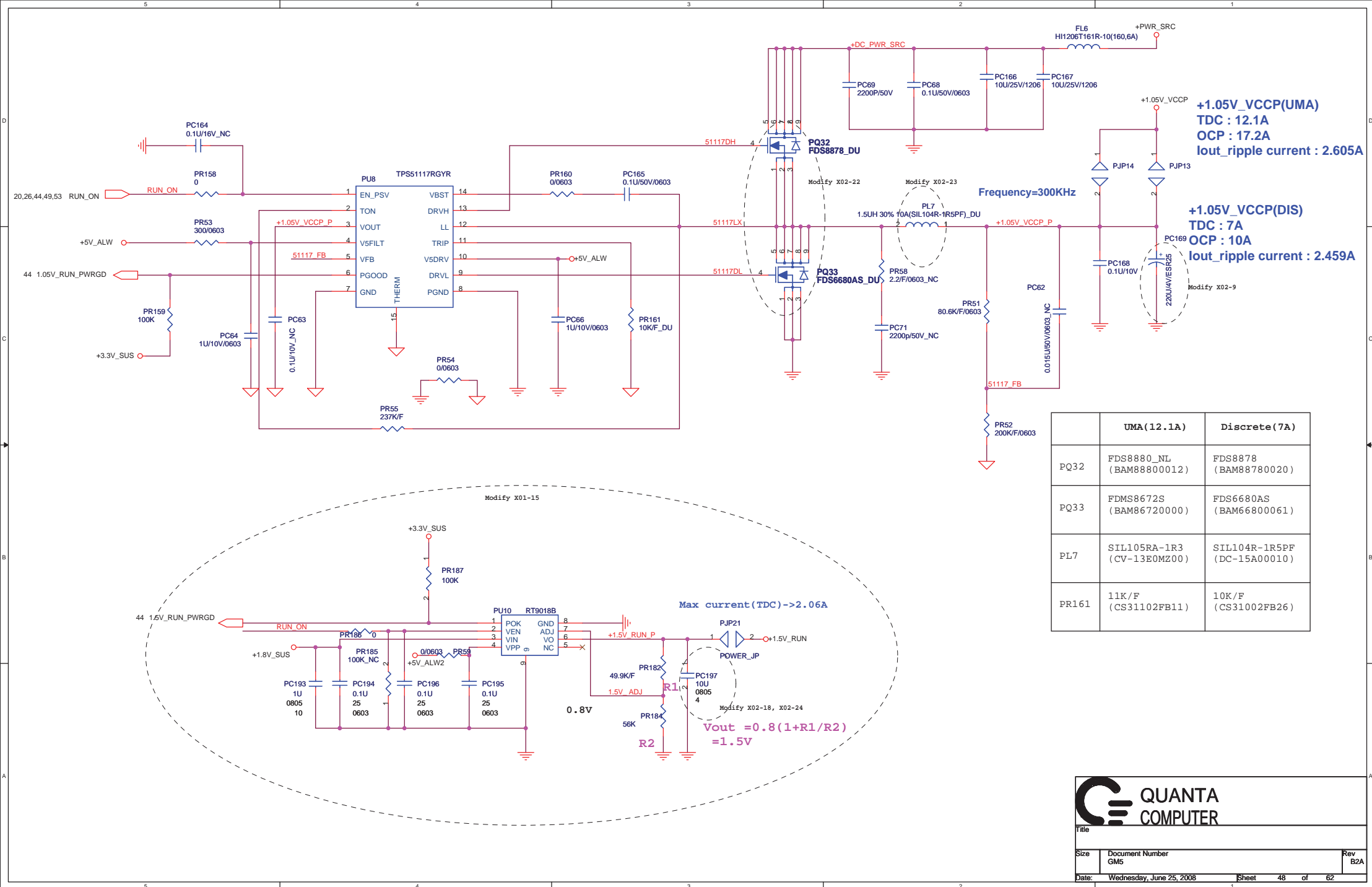


 QUANTA COMPUTER			
Title System Reset Circuit			
Size	Document Number GM5	Rev B2A	
Date	Wednesday, June 25, 2008	Sheet 44	of 62

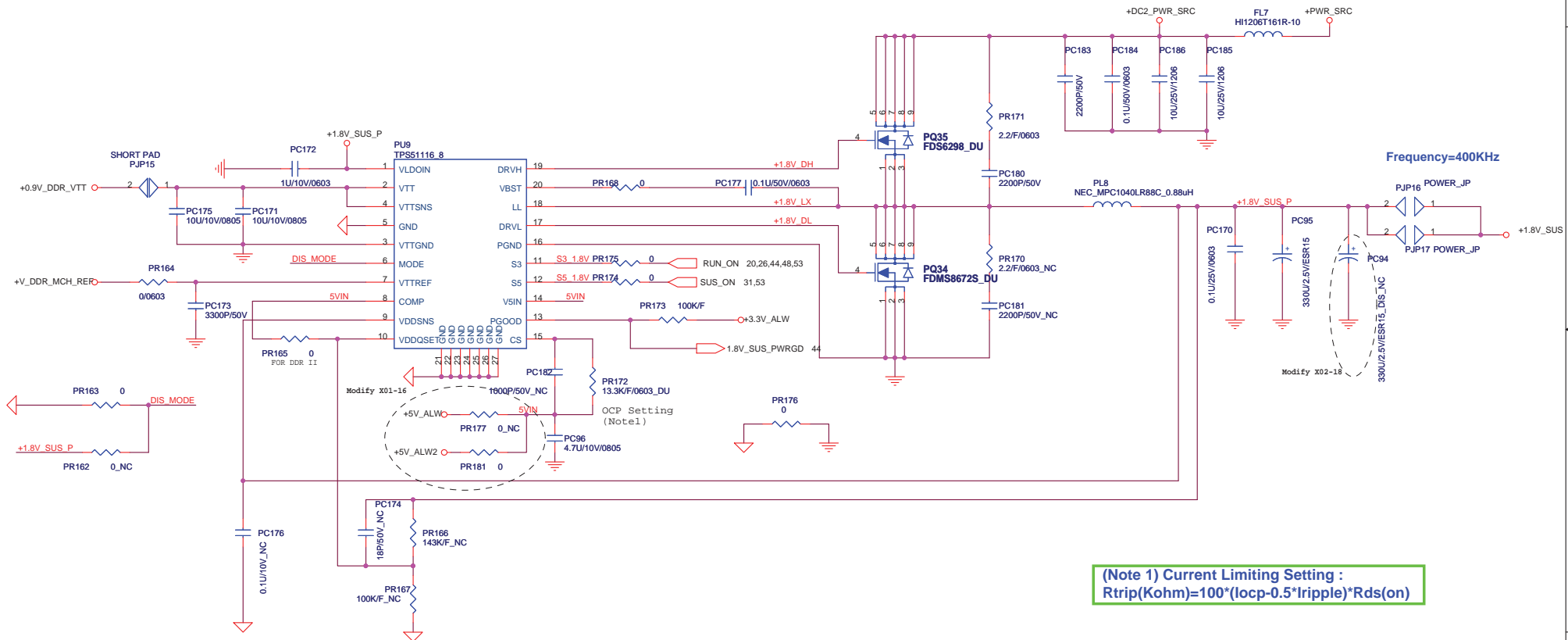


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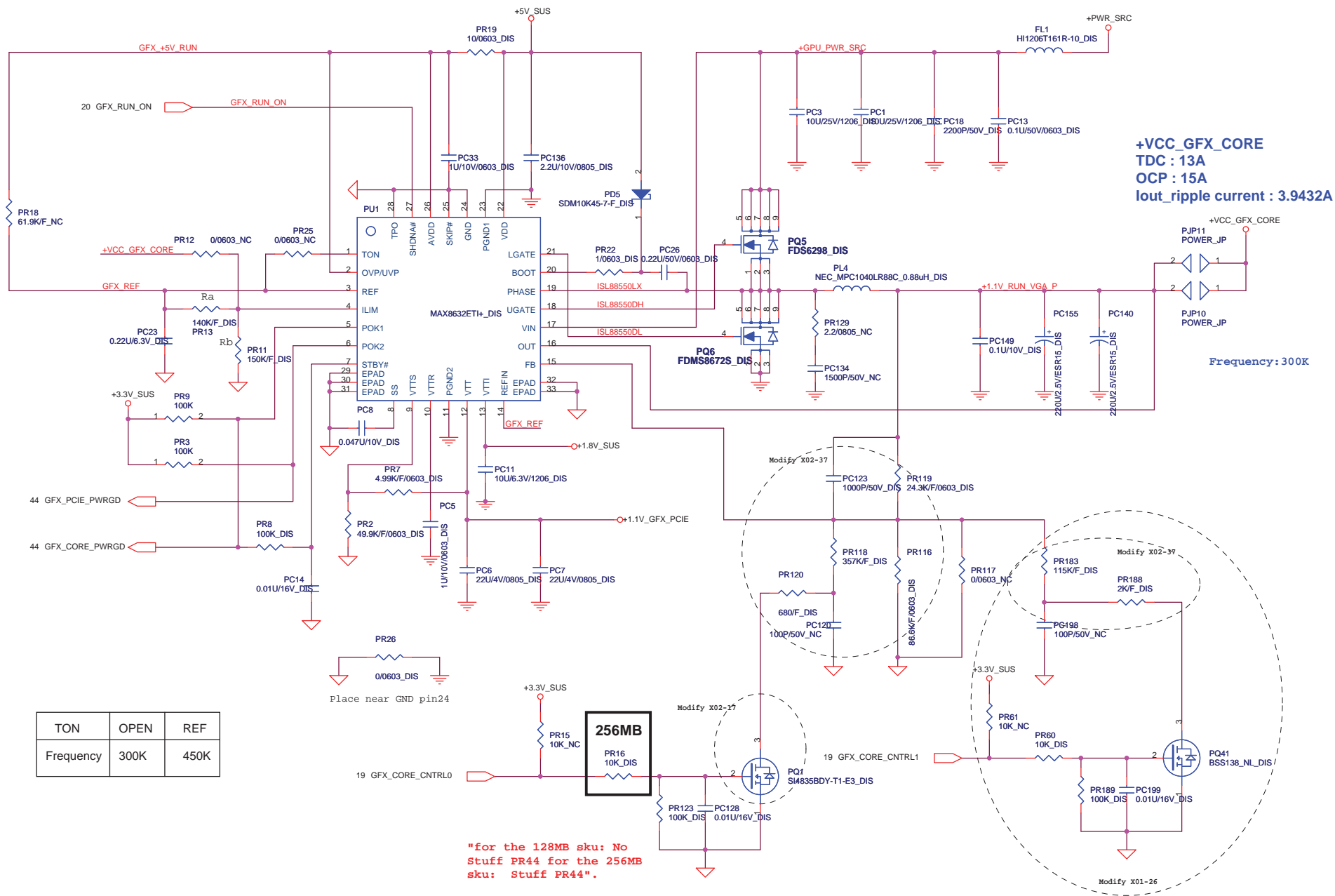
 QUANTA COMPUTER	
Title	
Size	Document Number
	GM5
Date	Rev
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Sheet 47 of 62	



+1.8V_SUS(UMA)
TDC : 10.25A
OCP : 14.9A
Iout_ripple current : 4.868A



(Note 1) Current Limiting Setting :
 $R_{trip}(K\Omega) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$



+VCC_GFX_CORE
TDC : 13A
OCP : 15A
lout_ripple current : 3.9432A

Frequency: 300K

TON	OPEN	REF
Frequency	300K	450K

"for the 128MB sku: No
Stuff PR44 for the 256MB
sku: Stuff PR44".

ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{DELTA} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

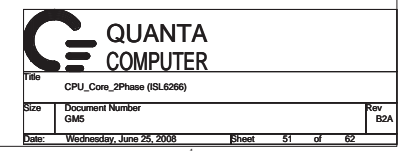
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.1V

QUANTA COMPUTER

Title: VGA DC/DC

Size: Document Number: GMS Rev: B2A

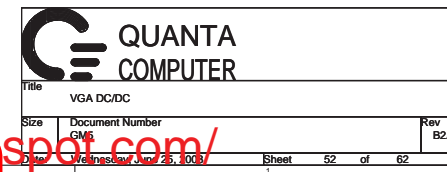
Date: Wednesday, June 25, 2008 Sheet: 50 of 62

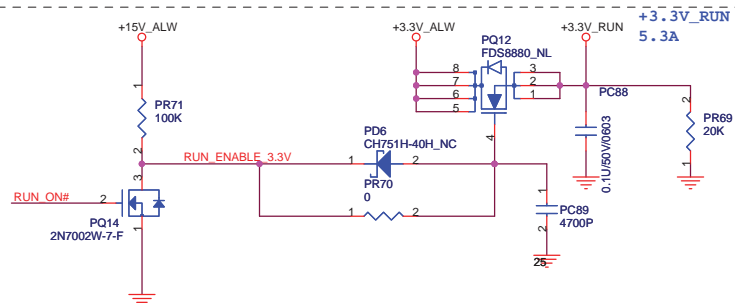
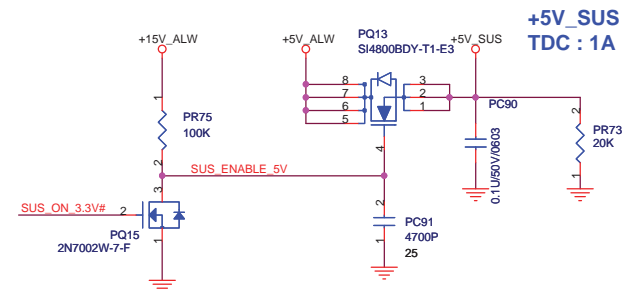
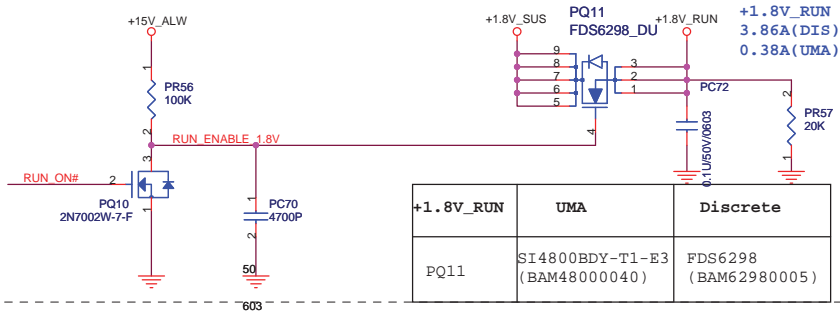
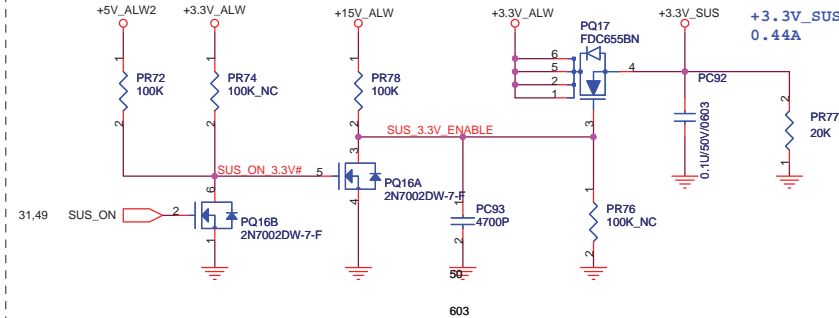
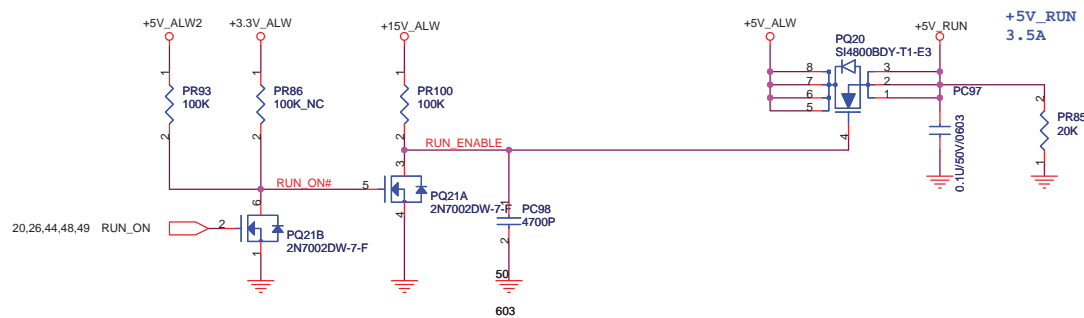


01-20, X02-36

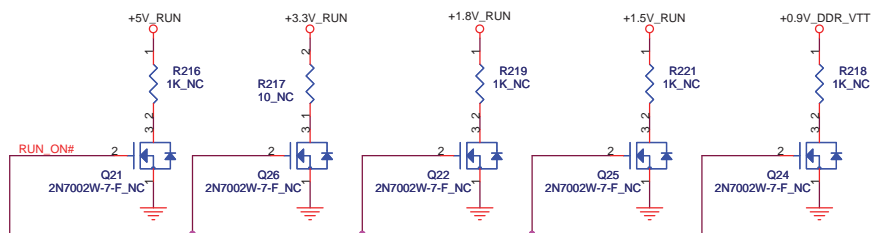
www.vinafix.vn

Size	Document Number
GM6	
Date	16/05/2007

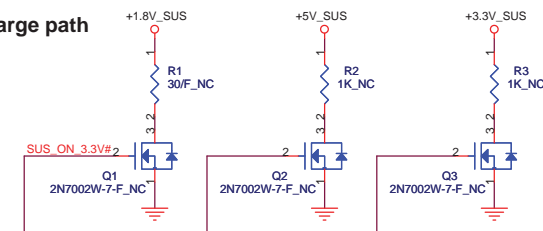




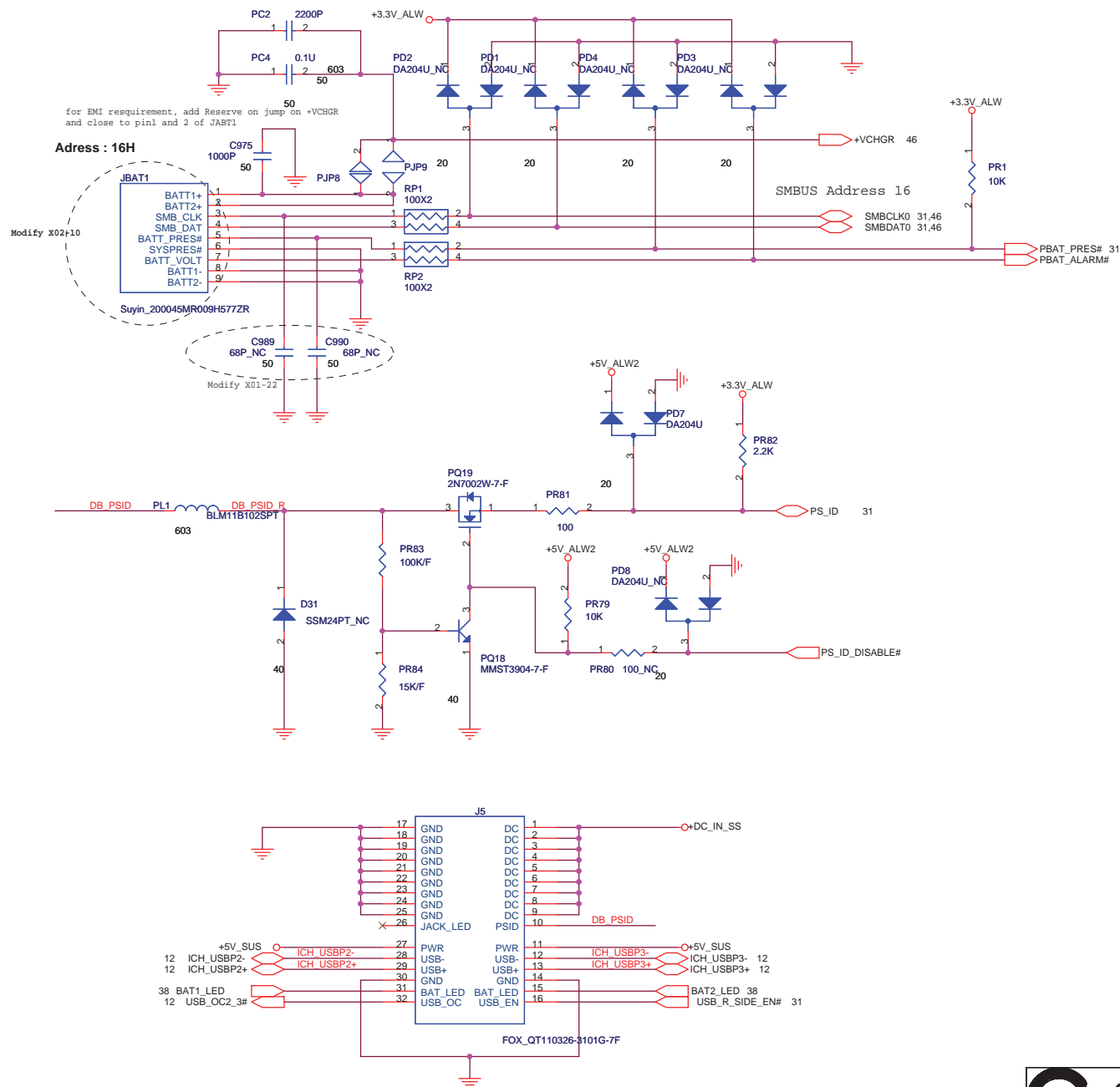
Reserve discharge path



Reserve discharge path



Title			RUN POWER SW
Size	Document Number	Rev	
	GM5	B2A	
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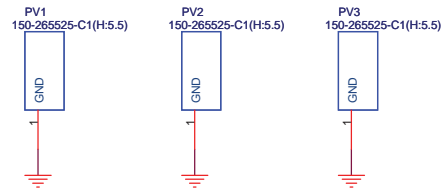
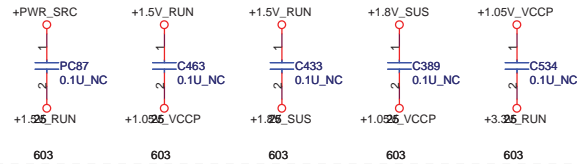


DCIN,BATT CONNECTOR

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Reserved for EMI.

Stitching caps



Page 26
SATA (HDD&CD_ROM)

Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

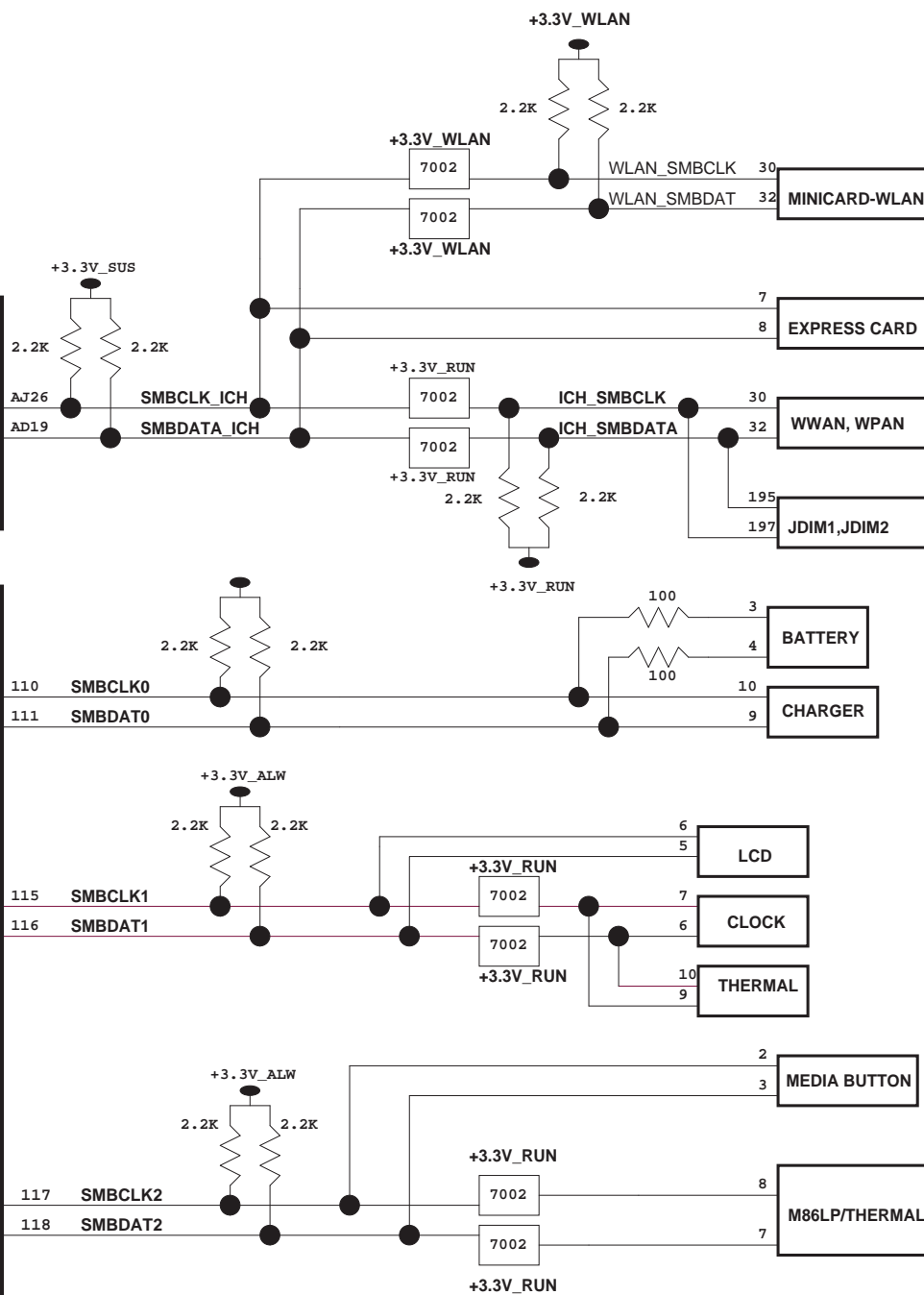
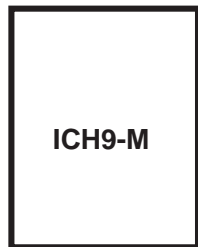
Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

Page 49
1.25V,1.8V,0.9V

Page 51
CPU_MAX8786(3phase)

Page 52
D/D Power



POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_RUN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

PCI TABLE

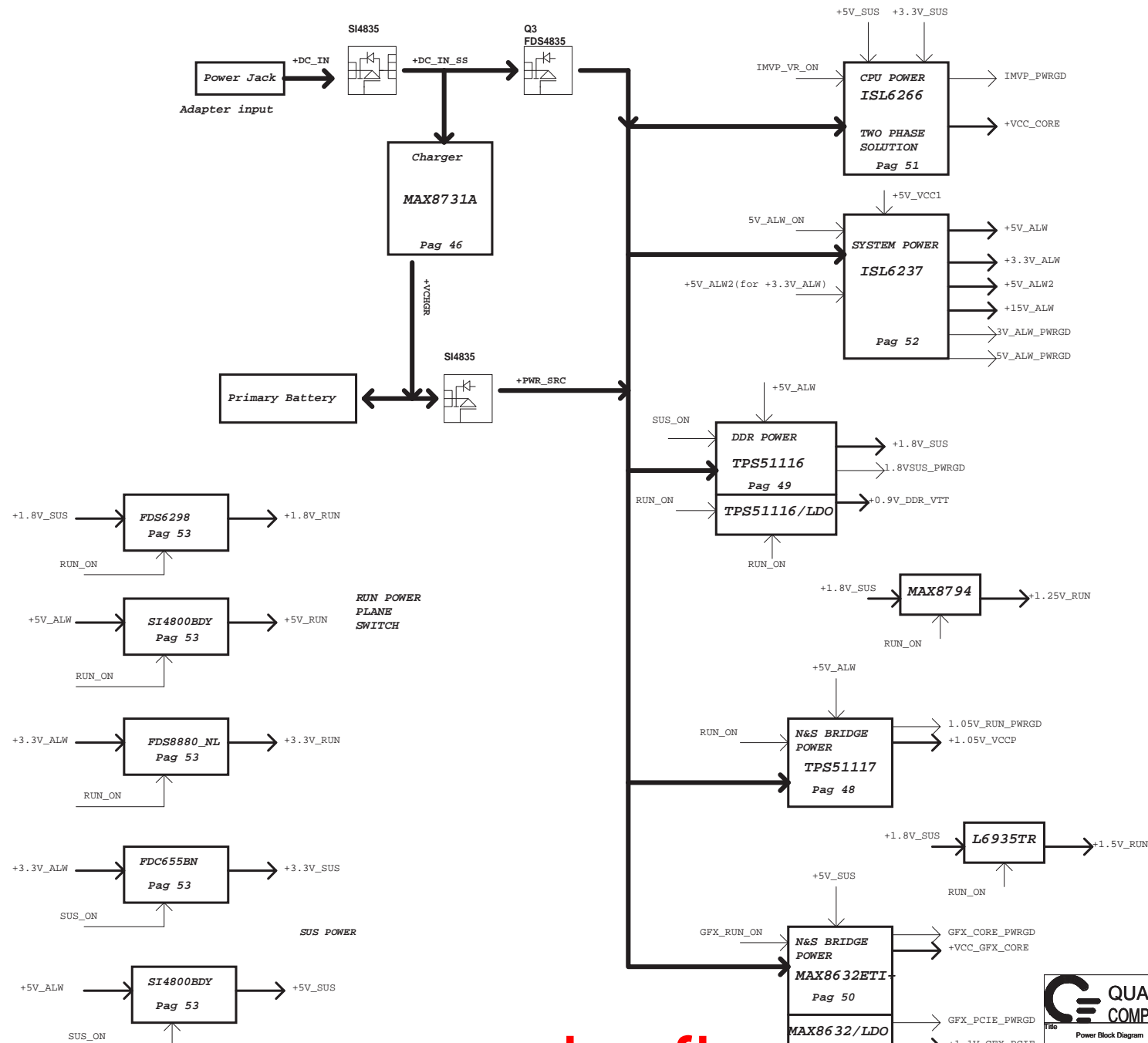
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#0 / GNT#0	PIRQB: 1394 PIEQD: Card reader

ICH9-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair bottom / left
	2	Side pair top/right(DB)
	3	Side pair Bot right(DB)
	4	WLAN
	5	Mini Card (WWAN)
	6	Mini Card (WPAN)
	7	Express Card
	8	USB W/ E-SATA port
	9	Reserved
	10	Biometric
ECE 5011	11	Camera
	1	None
	2	None
	3	None
ECE 5011	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

GM3 Power Design Block Diagram

2007/09/06




<http://laptop-motherboard-schematic.blogspot.com/>

Model	Rev	Page	Date	Rev.	Description
Pacino MV of Intel	1	25	6/6 2008		Change L54, L56, L70, L72 to CXCG900U00.
	2	43	6/6 2008		Change L80 to DB9FXLAN01.
	3	09	6/6 2008		Change D28 to BC01OKA5004.
	4	46	6/6 2008		Change PQ4, PQ24 to BAMA48350001.
	5	53	6/6 2008		Change PQ17 to BAMA4660102.
	6	25	6/11 2008		Reserve R999, R1000, R1001, R1002, C4945, C4946, C4947, C4948 for EMI solution.
	7	6	6/11 2008		Change R187, R213 pull high to +3.3V_RUN to solve backdrive in S3.
	8	14	6/11 2008		Change C957 from CH2220KMJ1 to CH71001MB82
	9	48	6/11 2008		Change PC169 from CH733KM826 to CH722KMT800
	10	54	6/11 2008		Change JBA71 from DFH09MR013 to DFH09MR019
	11	11-14	6/11 2008		Change U48 from AJQP220T05 to AJQ0T100T01
	12	35	6/11 2008		Change JUSB1 from DFH04FR126 to DFH511FR016
	13	4,8,9	6/11 2008		Change C96, C186, C243, C438 to CH71001MB82
	14	40	6/11 2008		Change J3 from DFH04MR040 to DFVWF04FR001
	15	38	6/11 2008		Change SW1 from DHL4LS12P03 to DHL4LS12P01
	16	35	6/11 2008		Change L17, L20, L50 from CXSG2T1001 to DC0900A014
	17	50	6/11 2008		Change PQ1 from BAMA00350000 to BAMA48350024
	18	21,48, 46,49	6/11 2008		NC PC131, PC129, PC197, PC34 depended on internal notice.
	19	25	6/11 2008		Change U13 to UMA part.
	20		6/11 2008		Delete reserved 0-ohm resistors: R192, R139, R226, R144, R145, R161, R248, R197, R198, R198, R188, R173, R195, R177, R209, R174, R196, R178, R215, R201, R176, R200, R179, R202, R175, R199, R180, R153, R152, R154, R140, R105, R228, R857, R717, R716, R241, R225, R206, R209, R210, R212, R245, R546, R847, R140, R848, R730, R842, R815, R871, R778, R769, R718, R664, R647, R665, R663, R705, R701, R700, R694, R142, R143, R77, R81, R75, R162, R195, R804, R767, R768, R683, R437, R547, R576, R575, R579, R428, R424, R422, R420, R423, R646, RPR14, PR4, PR6, PR97
	21	42	6/12 2008		Change R325 to 39K-ohm and R311 to 20K-ohm for LAN chip, BCM5794M.
	22	48	6/12 2008		Change PQ32 & PQ33 subsystem ID to PWR.Plane.Regulator_1p05v1p0v.
	23	46, 48	6/12 2008		Change PL3 to CV-5855T204 & PL7 to DC-15A00002.
	24	48	6/12 2008		Populate PC187 by power's request.
	25	14	6/12 2008		Change U53 to DELL PSL LDO part and schematic.
	26	40	6/13 2009		Change Audio codec U91 to revision C1, AL73C1X0B03 for ST build.
	27	25	6/13 2009		For HDMI pre-amp item, DCCCEFC Capacitance, add low-Capacitance MOSs on SMBUS between HDMI connector and PIV/DP411LS2DE.
	28		6/13 2009		Change C96, C98, C987, C438, C186, C243, C435, C595, C353, C957 to 220uF CAP2.0; CH722LM816.
	29	28	6/13 2009		Depopulate R819, because R5C833 don't need PME#.
	30	31	6/13 2009		Change the B10 to ST stage.
	31		6/13 2009		Change L87, L86, L91, L20, L17, L50, L46 to CXCG900U00.
	32	38	6/13 2009		Change SW1 to DHL4LS12P03
	33	41, 52	6/13 2009		Delete reserved 0-ohm resistors R826 and PR92.
	34	52	6/13 2009		Reserve a CAP PC200 for girth reducing of TEMP_FAIL.
	35	33	6/17 2009		Change C655 to 100uF CAP, CH7101MB800.
	36	19, 52	6/18 2010		DELL's request on thermal detect pin
	37	50	6/19 2010		Change PR119 to CS32433P915(0603), PR116 to CS3862F90A(0603), PR118 to CS48372F910(0402), R120 to CS16802F910(0603), PR185 to CS41152F909(0402), PR188 to CS2002F9B01(0402) to meet GPU core voltage step: 0.9V, 0.95V and 1.1V.
	38	3,4	6/23 2009		Change CPU socket(L42) PIN to DGT*6000001(Foxconn)
	39	3	6/23 2009		NC R116 for H_RESET# glitch.
	40	25	6/24 2009		Fine-tune the emphasis and the equalization of HDMI. 1. Pull OC1, OC2 to high and Pull OC1, OC3 to low. 2. Pull EC1_1 to low and pull EC1_2 to high.
	41	15	6/24 2009		Change JDM1 to Hx5.6mm connector, DGMK0000015 and JDM2 to H=10.1mm connector, DGMK0000016.
	42	31	6/26 2009		NC R601, R704 and populate R593 for activating platform reset signal.



	6		5		4		3		2		1
	Model	Item	Page	Date	Rev.	Description					
F	Pacino MV of Intel										
E											
D											
C											
B											
A											



QUANTA

COMPUTER

Title

A00 change list

Size

Document Number

Rev

GM3

B2A

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